INSTRUCTION MANUAL

MODEL 803
50 MHz PULSE/BURST GENERATOR

WAVETEK

WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123

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50 MHz PULSE/BURST GENERATOR

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SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

The instrument power receptacle is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference: ⏚ or ⚠ stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.

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SECTION 1
GENERAL DESCRIPTION

1.1 THE MODEL 803

The Model 803 is a 50 MHz general purpose laboratory pulse generator with triggered burst. The instrument gives you full control in primary pulse triggering and shaping plus simultaneous TTL, $\overline{\text{TTL}}$ and sync pulses. The primary pulse output has controllability in rate, width, delay, upper level, lower level and a choice of positive, negative or complementary outputs. The TTL and $\overline{\text{TTL}}$ are of fixed levels and rise times that are standard for use with compatible devices. The primary pulse has rise and fall times of 5 ns or less.

Pulses may be output continuously or triggered for a single pulse, a counted burst of pulses or a timed gating of pulses. Double pulses can be selected to occur for each single pulse above.

The output is ±10 volts with a 50Ω termination. Upper and lower pulse levels are fully adjustable through ±10 volts, a 20 volt window. Termination may be internal, at the load or both.

1.2 SPECIFICATIONS

1.2.1 Versatility

Four Simultaneous Pulse Outputs

Fixed TTL level sync, TTL and $\overline{\text{TTL}}$ outputs, and variable output pulses are available over a 5 Hz (200 ms) to 50 MHz (20 ns) frequency range.

For optimum pulse characteristics from the variable amplitude pulse output, an internal 50Ω load can be selected via a front panel control.

Operational Modes

Continuous: Generator oscillates continuously at selected frequency.

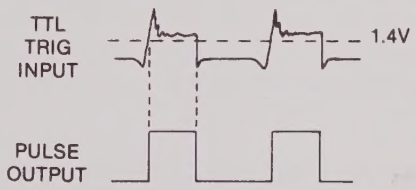
Triggered: Generator quiescent until triggered by external TTL pulse or front panel control, then generates one pulse.

Gated: Generator oscillates at the period rate selected by the front panel control when gate input is high. Generator quiescent when input is low. First cycle is synchronous with rising edge of gating signal.

Burst: Generator oscillates at the period or rate selected by the front panel control for a specified number of cycles when triggered by external TTL pulses or front panel manual trigger.

Double Pulse: Same as continuous, triggered, and burst, except two pulses occur for each period. Time to second pulse is controlled by delay control. Double pulse occurs at all outputs except sync.

External Width: External signal at trigger input determines output pulse width and period as shown.



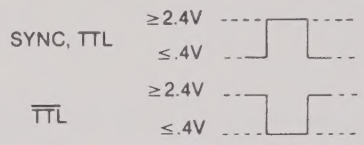
1.2.2 Pulse Outputs

Variable Amplitude Pulse

SOURCE	LOAD	DYNAMIC RANGE	AMPLITUDE MAXIMUM	AMPLITUDE MINIMUM
50Ω	50Ω	+5V −5V	5V	0.5V
1 kΩ	50Ω	+10V	10V	1V
OR				
50Ω	≤1 kΩ	−10V		

Upper and lower pulse levels are independently adjustable. Pulse dynamic range is ±10V when load is 50Ω terminated and source is not (internal 50Ω off) or vice versa. Maximum pulse amplitude is 10V; minimum is 1V. Dynamic range and pulse amplitude are decreased by a factor of 2 when source and load are 50Ω terminated. Overshoot and ringing are less than (±5% of amplitude setting + 100 mV) when terminated into 50Ω at both load and source. Transition times are less than 5 ns.

Sync, TTL and $\overline{\text{TTL}}$ Pulses
Sync pulse levels from 50Ω; TTL and $\overline{\text{TTL}}$ pulse levels into 50Ω termination.



Transition times less than 7 ns into 50Ω termination.

Normal/Complement Control
Normal pulse or its complement is selected. The normally quiescent and active levels are reversed in complement format. This control affects all outputs except sync pulse.

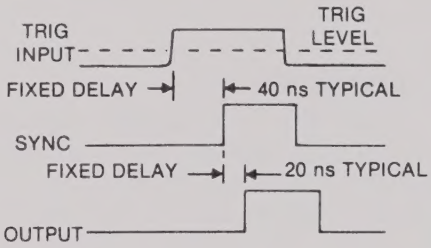
1.2.3 Time Domain

Period
Period range is from less than 20 ns to greater than 200 ms in 7 overlapping ranges. Period jitter is less than ±0.1% plus 50 picoseconds.

Width
Width range is from less than 10 ns to 10 ms in 6 overlapping ranges. Maximum duty cycle is 70% for periods to 200 ns, decreasing to 50% for 20 ns periods. Width selector switch also has a square wave detent and a customer-specified detent.* ⊓ duty cycle is 50 ±4% to 2 μs period, changing to 50 ±15% at 20 ns period. Width jitter is less tthan ±0.1% plus 50 picoseconds. Sync pulse duty cycle is 50 ±4% of pulse period to 2 μs period, changing to 50 ±15% at 20 ns period except in trigger and external width modes, in which case it is determined by the trigger signal.

Delay
Pulse occurrence can be delayed from less than 10 ns to 10 ms with respect to the sync pulse (not including fixed delay). Delay selector switch also has a customer-specified detent.* Maximum delay duty cycle is 70% for periods to 200 ns, decreasing to 30% for 20 ns periods.

Delay jitter is less than ±0.1% plus 50 picoseconds. Fixed delay is as shown.



Burst
Burst count of 1 to 99,999 is front panel selectable. Maximum pulse frequency in burst mode is 20 MHz. Burst trigger source is manual or external. Minimum external burst trigger width is 25 ns.

1.2.4 Input Characteristics

External Trigger
The circuit receiving the external trigger is TTL compatible. Triggering level is fixed at approximately 1.4V. Input impedance is greater than 500Ω shunted by approximately 33 pF. Triggering and gating occurs on the rising edge of the input signal.

1.2.5 General

Environmental
Specifications apply at 25°C ±5°C after 30 minutes warm-up. Instrument will operate from 0°C to 50°C.

Dimensions
28.8 cm (11.4 in.) wide; 13.3 cm (5¼ in.) high; 29 cm (11.4 in.) deep.

Weight
4.0 kg (8.9 lb) net; 5.4 kg (12 lb) shipping.

Power
108 to 132V or 216 to 250V; 50 to 400 Hz; 40 watts nominal.

**Customer-installed capacitor determined detent range.*

SECTION 2
INSTALLATION

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earthground path can be identified at the plus on the instrument power cord; of the three terminals, the earth ground terminal is the nonmatching shape usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 108 to 126 Vac line suply and with a 0.6 amp fuse.

Conversion to other input voltages require a change in rear panel fuse-holder voltage card position and fuse according to the following table and procedure.

Card Position	Input Vac	Fuse (Slow Blow, 3 AG)
100	90 to 105	0.6 amp
120	108 to 126	0.6 amp
220	198 to 231	0.3 amp
240	216 to 250	0.3 amp

1. Open fuse holder door and rotate FUSE PULL to left to remove the fuse.
2. Select operating voltge by orienting the printed circuit board to position the desired voltage on the top left side. Push the board firmly into its module slot.
3. Rotate the FUSE PULL back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.
4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

2.2.2 Signal Connections

Use 2 foot RF58U 50Ω shielded cables equipped with female BNC connectors to distribute input and output signals when connecting this instrument to associated equipment.

2.3 ELECTRICAL ACCEPTANCE CHECK

This checkout procedure verifies the generator operation. If a malfunction is found, refer to the Warranty in the front of this manual. A 2 channel oscilloscope and 50Ω coax cable are needed for this procedure (see figure 2-1).

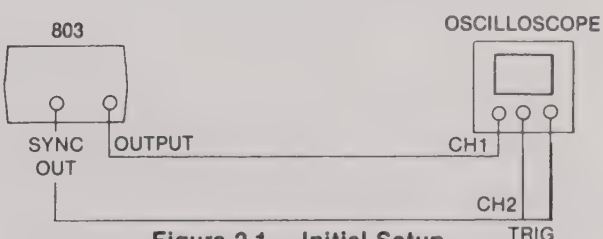


Figure 2-1. Initial Setup

Preset the pulse generator controls by setting the following switches to their white mark:

PERIOD/RATE
DELAY
WIDTH

Set the PULSE MODE switches OFF except set INT 50Ω ON.

Set the BURST/CONT/GATE switch to CONT.

Set BURST length to 00005.

Set the following controls to 12 o'clock:

PERIOD/RATE VERNIER
DELAY VERNIER
WIDTH VERNIER
LOWER LEVEL
UPPER LEVEL

Perform the steps in table 2-1. Only approximate values are required to verify operation.

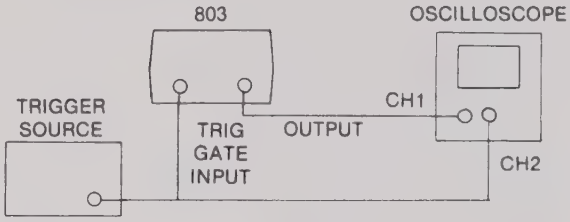


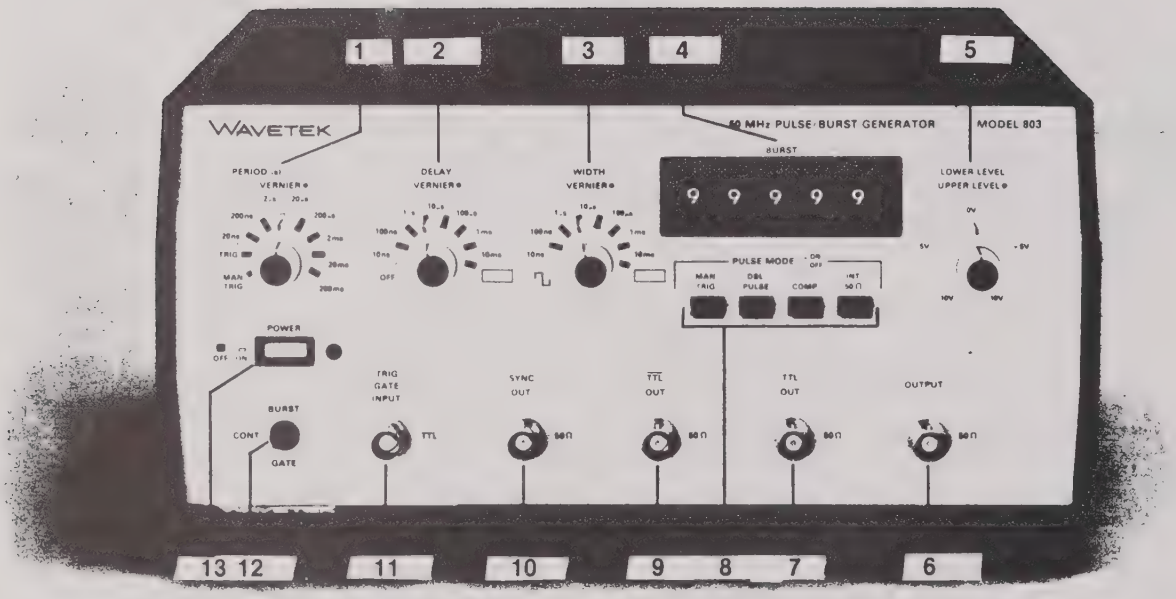
Figure 2-2. Second Setup

Table 2-1. Performance Checkout

Step	Control	Position/Operation	Observation
1	POWER	ON	CH 1: A near 0 volt dc level. (LEVEL control is not calibrated.) CH 2: Approximately 2.5 volt pulses.
2	LOWER LEVEL	Rotate ccw	Pulse base drops 10V.
3	UPPER LEVEL	Rotate ccw	Pulse upper level drops 10V.
4	UPPER LEVEL	Rotate cw. Make observation; then reposition for good display	Pulse rises 10V, then rises 10V more while pulling the base up 10V. Base rises to 0V.
5	COMP	ON then OFF	Set scope for one or two cycles. Observe the switching of duty time from first half cycle to second half cycle.
6	WIDTH	Rotate to 1 μs | 10 μs	Pulse width changes.
7	WIDTH VERNIER	Rotate ccw.	Pulse width decreases.
8	DELAY	Rotate ccw.	Pulse width decreases.
9	DELAY VERNIER	Rotate ccw, cw, then to 12 o'clock.	Pulse delay moves to left, then right.
10	PERIOD/RATE VERNIER	Rotate cw, then to 12 o'clock	Period increases, then decreases.
11	DBL PULSE	ON	Two pulses instead of one.
12	DELAY VERNIER	Rotate ccw, then cw, but maintain double pulse, return to 12 o'clock.	Pulse pairs move closer, then further apart.
13	WIDTH VERNIER	Rotate to 12 o'clock, but maintain double pulse.	Pulse width of each pulse of pulse pair increases.
14	OUTPUT	Remove cable; place on TTL out connector.	TTL double pulse output.
15	TTL OUT	Remove cable; place on $\overline{\text{TTL}}$ out connector.	$\overline{\text{TTL}}$ double pulse output complement of previous output.

Table 2-1. Performance Checkout (Continued)

Step	Control	Position/Operation	Observation
Change to setup in figure 2-2; trigger with a 10 kHz square wave signal; adjust scope for best display.			
16	BURST/CONT/ GATE WIDTH DBL PULSE PERIOD/RATE	 GATE 1 μs 10 μs OFF TRIG	(Trigger on CH2.) A single pulse on CH1 coincident with square wave on CH2.
17	PERIOD/RATE MAN TRIG Switch	MAN TRIG Push and release	(Trigger on CH1.) A single pulse on CH1; repeated operation of the MAN TRIG switch makes pulse observable.
18	BURST/CONT/ GATE PERIOD/RATE DELAY WIDTH	 BURST 200 ns μs OFF ⊓⊔ (square wave)	(Trigger on CH2.) A burst of 5 pulses on CH1 coincident with square wave on CH2.
19	BURST/CONT/ GATE	GATE	Pulse burst on CH1 whose width coincides with positive level width of CH2's square wave.



NOTE: Major Modes of operation are:

- Continuous
- Externally Triggered
- Manually Triggered
- Externally Gated
- Manually Gated
- External Width
- Externally Triggered Burst
- Manually Triggered Burst

Refer to paragraph 3.2.1

Figure 3-1. Controls and Connectors

SECTION 3
OPERATION

3.1 CONTROLS AND CONNECTORS

The generator controls and connections are shown in figure 3-1 and keyed to the following descriptions.

1 **PERIOD/RATE Switch** — Selects one of seven ranges of pulse period calibrated in seconds and hertz (for use in continuous, gated and burst modes, where internally generated periods are required). The TRIG detent selects the externally triggered one pulse (or one double pulse) mode. The output is held at the inactive level until a TTL level trigger signal is applied at the TRIG GATE INPUT BNC. On the input rising edge, one pulse (or one double pulse) is output. The MAN TRIG detent selects the manually triggered (one pulse or one double pulse) mode. Manual/mode is the same as external mode except pressing the MAN TRIG switch generates the output.

VERNIER Control — Varies the pulse period within the range selected by the outer knob. Clockwise increases the pulse period and decreases frequency.

2 **DELAY Switch** — Selects one of seven ranges of pulse delay or time-to-second-pulse of double pulses in continuous, triggered, gated, or burst modes. OFF position of DELAY switch ensures minimum delay. The unmarked detent is for customer selected range.

VERNIER Control — Varies the delay time within the range selected by the outer knob. Clockwise increases the delay.

3 **WIDTH Switch** — Selects one of seven ranges of pulse width or an approximate 50% duty cycle. The unmarked detent is for customer selected range.

VERNIER Control — Varies the pulse width within the range selected by the outer knob, except when outer knob is set at ⊓ .

4 **BURST Switch** — Sets the exact number of pulses, between 1 and 99 9999, in a burst. (Note that setting 00000 equals 00001, a single-pulse burst.)

5 **LOWER LEVEL Control** — Outer knob sets the lower level of the OUTPUT pulse, which may be varied from −10 to +10 volts into a single 50Ω termination or −5 to +5 volts into a double 50Ω termination. Maximum pulse heights are 10 and 5 volts, respectively.

UPPER LEVEL Control — Inner knob sets the upper level of the OUTPUT pulse. Upper level range is identical to that stated for the lower level.

6 **OUTPUT Connector** — The main output of the generator. Pulses from this output may be controlled in level as well as frequency and width.

7 **TTL OUT Connector** — An output with a transistor-transistor-logic level pulse whose occurrence and duration are controllable. Normal pulse level is <0.4V quiescent, >2.4V active into a 50Ω termination. Levels are reversed for the complement pulse.

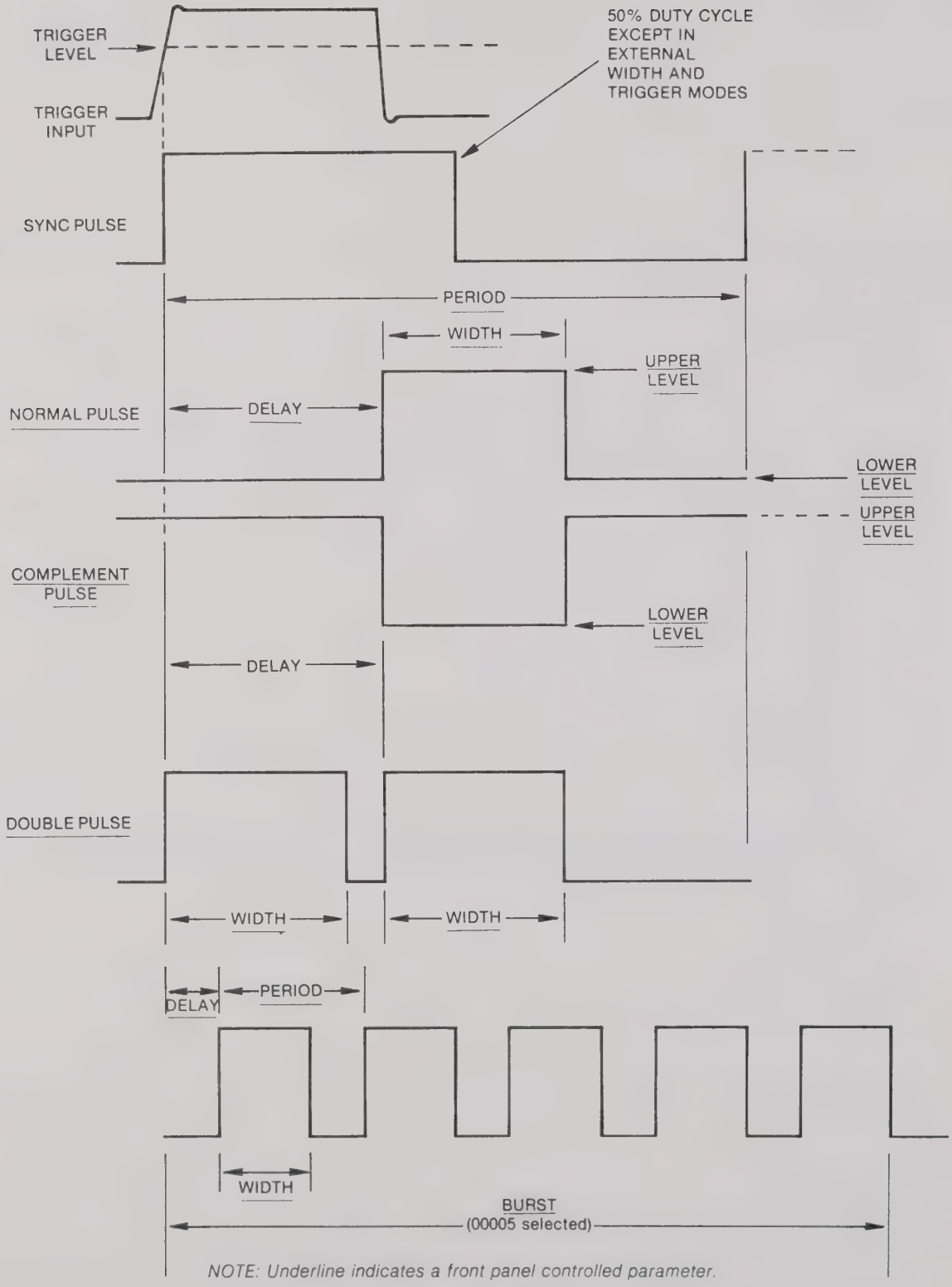
8 **PULSE MODE Switches**

NOTE

These switches do not select the major modes of operation. (Refer to paragraph 3.2.1).

MAN TRIG — Triggers the generator when pressed. Can be used in all modes except continuous and external trigger. Output depends on the mode selected (ref: paragraph 3.2.1).

DBL PULSE Switch: When ON, a double pulse occurs where one pulse would occur when OFF. (External width mode is not affected.) Time to leading edge of second pulse is controlled by the DELAY setting. In burst mode, the number of pulses is double the BURST switch selection.



NOTE: Underline indicates a front panel controlled parameter.

Figure 3-2. Pulse Parameters

COMP Switch — Selects a normal pulse when OFF or its complement when ON, which swaps the active and quiescent levels. Affects all outputs, except SYNC.

INT 50Ω Switch — When ON, the output current source is 50Ω terminated internally. When OFF, the current source has greater than 1 kΩ impedance.

9 **$\overline{\text{TTL}}$ OUT Connector** — An output like the TTL output **7** except active and quiescent levels are reversed.

10 **SYNC OUT Connector** — A TTL level output from a 50Ω source. Square wave in all modes except external width and externally triggered modes, in which pulse width is determined by trigger pulse width.

11 **TRIG GATE INPUT Connector** — Accepts an external TTL level signal to trigger or gate the generator. Triggers on rising edge of input. Gates off when level is at a TTL low level. If the BURST/CONT/GATE switch is set to GATE, the TRIG GATE INPUT BNC must be at a TTL low, shorted or terminated with a 50Ω load; otherwise the generator will run continuously.

12 **BURST/CONT/GATE Switch** — Selects either the triggered burst, continuous, or gate mode. For manually triggered or externally triggered single pulse (or double pulse) or external width modes refer to 1. For operation in the various modes, refer to paragraph 3.2.1.

13 **POWER Switch** — Pulse generator on/off switch features red power-on indicator light and black/white changing switch surface for off/on indication.

3.2 OPERATION

3.2.1 Modes of Operation

The following modes of operation are available and selectable as described herein.

Paragraph	Major Mode of Operation
3.2.1.1	Continuous
3.2.1.2	Externally Triggered
3.2.1.3	Manually Triggered
3.2.1.4	Externally Gated
3.2.1.5	Manually Gated
3.2.1.6	External Width
3.2.1.7	Externally Triggered Burst
3.2.1.8	Manually Triggered Burst
	Other
3.2.1.9	Double Pulses

In continuous mode, sync on the SYNC OUT BNC. In all other modes, sync on the trigger signal. See figure 3-2 for pulse parameters.

Observe the following constraints:

Delay ≤70% of period.
Width ≤70% of period.

3.2.1.1 Continuous

For a continuous stream of pulses, set the controls (and connectors) as follows:

Control	Operation
BURST/CONT/ GATE Switch	CONT
INT 50Ω Switch	ON
PERIOD Switch	Any position except TRIG or MAN TRIG
Other Controls	Set as desired

3.2.1.2 Externally Triggered

For a pulse, or pulse pair, triggered by an external signal, set controls (and connectors) as follows:

Control	Operation
BURST/CONT/ GATE Switch	Switch CONT or GATE
TRIG/GATE INPUT Connector	Apply TTL pulse
INT 50Ω Switch	ON
WIDTH Switch	Set to range desired (but not ⊓)
Other Controls	Set as desired

Triggering occurs on the trigger pulse rising edge.

3.2.1.3 Manually Triggered

For a pulse, or pulse pair, triggered by the MAN TRIG switch, set control (and connectors) as follows:

Control	Operation
BURST/CONT/ GATE Switch	CONT or GATE
PERIOD Switch	MAN TRIG
INT 50Ω Switch	ON
WIDTH Switch	Set to range desired (but not ⊓)
Other Controls	Set as desired

3.2.1.4 Externally Gated

For continuous pulses for the duration of the positive level of the gate signal, set controls (and connectors) as follows:

Control	Operation
BURST/CONT/ GATE Switch	GATE
PERIOD Switch	Any position except TRIG or MAN TRIG
TRIG GATE INPUT Connector	Apply TTL pulse
INT 50Ω Switch	ON
Other Controls	Set as desired

3.2.1.5 Manually Gated

For continuous pulses each time the MAN TRIG Switch is pressed, set controls (and connectors) as follows:

Control	Operation
BURST/CONT/ GATE Switch	GATE
PERIOD Switch	Any position except TRIG or MAN TRIG
TRIG GATE INPUT Connector	Connect at 50Ω termination or short
INT 50Ω Switch	ON
MAN TRIG Switch	Push to gate generator
Other Controls	Set as desired

3.2.1.6 External Width

For pulses whose widths are determined by an external signal, set the controls as for externally triggered (paragraph 3.2.1.2), except the WIDTH switch must be set to ⊓ .

3.2.1.7 Externally Triggered Burst

For a pulse burst, triggered by an external trigger, set the controls (and connectors) as follows:

Control	Operator
BURST/CONT/ GATE Switch	Burst
PERIOD Switch	Any position except MAN TRIG or TRIG
BURST Switch	Set to desired burst length
TRIG GATE INPUT	Apply TTL Pulse
INT 50Ω Switch	ON

3.2.1.8 Manually Triggered Burst

For a pulse burst, triggered by the MAN TRIG Switch, set the controls as for BURST except remove the TRIG GATE INPUT signal and press MAN TRIG to trigger the burst.

3.2.1.9 Double Pulses

For double pulses in any mode, set the additional controls as follows:

Control	Operation
DBL PULSE	ON
DELAY	Set for desired time between start of first pulse and second pulse of pulse pairs. (Since the same one-shot forms both pulses, a minimum recovery time is necessary.)

3.2.2 White Marks

When first becoming familiar with the 803, the white mark settings are handy. The white mark settings for the front panel switches will always give a 50 to 500 kHz sync signal when power is on. The same settings will give 50% duty cycle TTL, $\overline{TTL}$ and output pulses; the LOWER LEVEL/UPPER LEVEL control may need adjusting to observe the output on an oscilloscope. Once the output is observed, each control can be adjusted and observed until the desired result is obtained.

3.2.3 Pulse Width and Delay

Narrow duty cycle pulses require a normal output (COMP OFF) while greater than 70% duty cycle pulses require the COMP ON setting to allow the width circuitry sufficient recovery time. When using DELAY time, ensure that delay is $\leq$70% of PERIOD and width is $\leq$70% of PERIOD.

The ⊓ width setting gives a 50% duty cycle in continuous mode, when TRIG or MAN TRIG is selected on the PERIOD switch, the pulse width is determined by the trigger signal width. This is external width mode of operation.

Table 3-1. Capacitance and Range

Delay or Width Range	Capacitance
10 ns - 100 ns	None
100 ns - 1 μs	2000 pF
1 μs - 10μs	0.02μF
10μs - 100μs	0.2μF
0.1 ms - 1 ms	2.0 μF
1 ms - 10 ms	20 μF
10 ms - 100 ms	200 μF
0.1s - 1s	2000 μF

The unmarked detent on the DELAY switch and WIDTH switch can be any desired range by placing appropriate capacitors on the circuit board, as shown

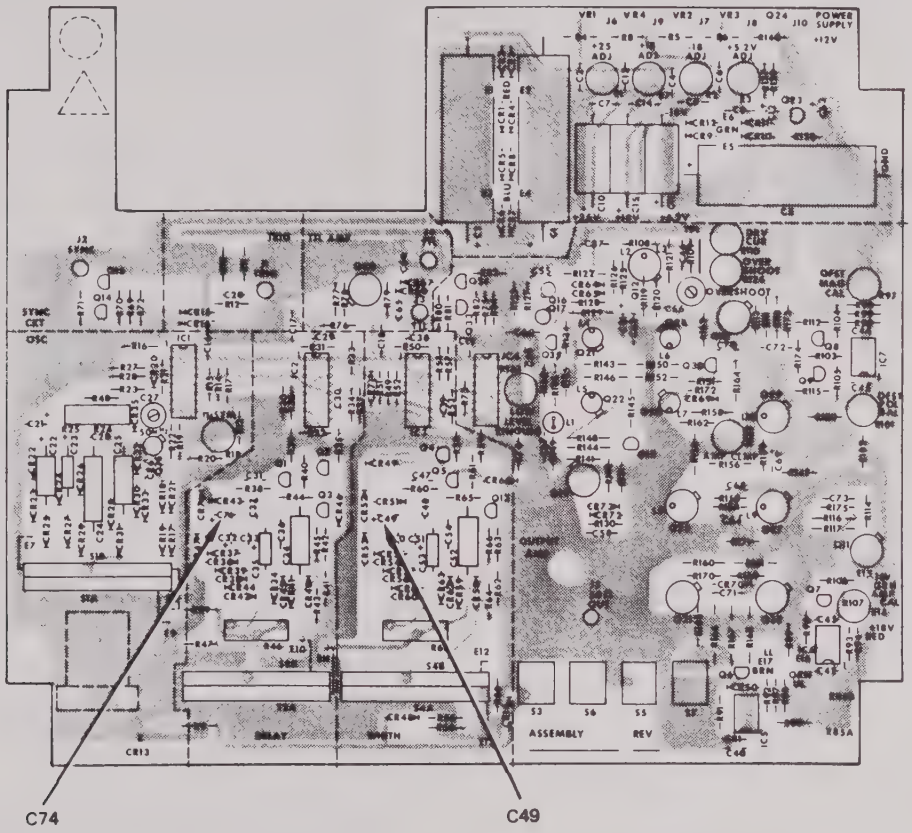


Figure 3-3. Placement of Customer Option Capacitors

in figure 3-3. Refer to table 3-1 for typical capacitance and range.

SOURCE	LOAD	DYNAMIC RANGE	Amplitude	
			Maximum	Minimum
50Ω	50Ω	+ 5V – 5V	5V	.5V
*1kΩ OR 50Ω	50Ω ≥ 1kΩ	+ 10V – 10V	10V	1V

*1 kΩ is the unterminated source impedance of the OUTPUT.

Figure 3-4. Load and Source Terminations

3.2.4 Output Terminations

Only 50Ω RG58U cables should be used to connect the 803 to the circuit under test. Either the INT 50Ω should be ON or a 50Ω 2W load should be used at the circuit end of the cable. For best pulse fidelity, a 50Ω load at both the source and the load is required.

As shown in figure 3-4, the combinations of load and source impedances determine the output pulse amplitude range and the dynamic range. As shown, when a greater than 5V pulse is desired, only one 50Ω termination can be used, and the placement of the termination can optimize the pulse purity. In this case, the capacitance of the circuit being driven must be considered. For capacitive loads greater than 20 pF, reflections on the line are most effectively absorbed by the 50Ω termination at the 803 (INT 50Ω switch ON). For capacitive loads less than 20 pF, the 50Ω termination should be placed at the load side of the line. When a less than 5V pulse is required, a 50Ω termination at each end of the line is recommended for optimum pulse purity.

The 50Ω terminations should always be used on the SYNC, TTL and $\overline{\text{TTL}}$ outputs.

3.2.5 Duty Cycle

Always use the lowest range possible for both delay and width functions. This will reduce the recovery time of the circuit one-shots and extend the maximum duty cycle of the 803 to its fullest capability.

3.2.6 Output Mixing

By triggering a second 803 from the sync output of the first 803 and then mixing their outputs in a common load, three level signals can be created, as shown in figure 3-5.

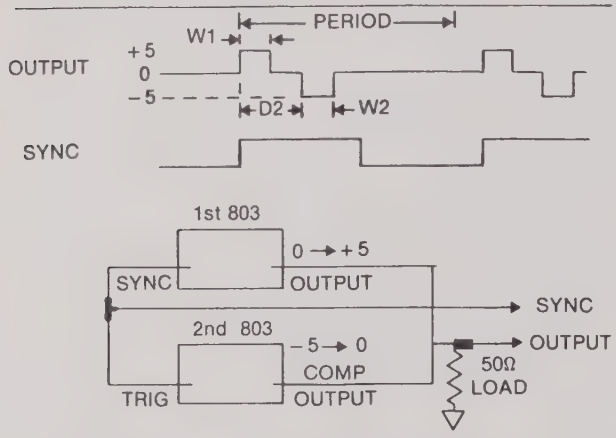


Figure 3-5. Output Mixing

3.2.7 Precise Output Levels

Many times when testing a circuit, it is desirable to lock the output of the generator at either the high or low level. A precise measurement of this level may then be obtained using a DVM.

To lock the output at high or low level, select EXT TRIG and ⎍ with no TRIG GATE INPUT. Use the COMP ON/OFF switch to select high and low level outputs.

3.2.8 Fixed Delay

A fixed delay of 20 ns has been incorporated within the 803 to ensure that the leading edge is visible on the scope. If this delay is not desired, simply increase the length of the sync cable coax at the rate of 1.5 ns/ft to obtain the desired result.

3.2.9 Two Phase Clocking

If a secondary 803 is triggered by the sync out from the primary 803, a two phase nonoverlapped clock source can be obtained as shown in figure 3-6.

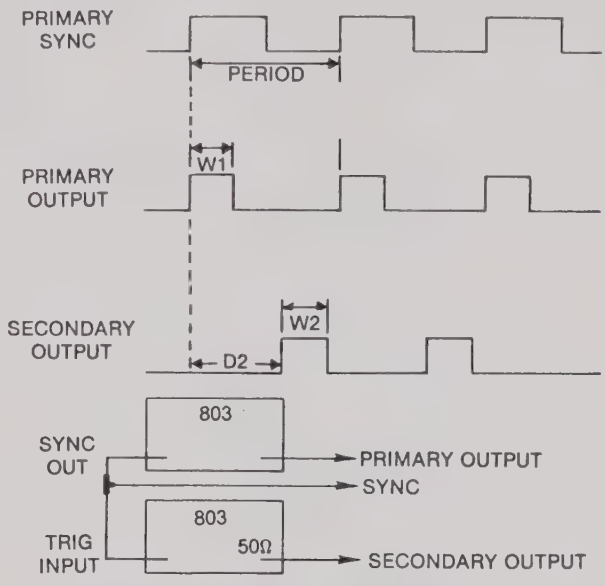


Figure 3-6. Two Phase Clock Generation

3.2.10 Rise Time Measurements

When measuring rise time in a linear device under test, the error induced by the rise time of the testing system must be considered. For example, when observing the 803 rise time on an oscilloscope, 803 rise time is

$$t^2_{observed} = t^2_{scope} + t^2_{803}$$

or

$$t_{803} = \sqrt{t^2_{observed} - t^2_{scope}}$$

That is, the observed rise time must be corrected for by the inherent oscilloscope rise time to determine the actual 803 rise time. Extending the method to include a circuit under test will determine circuit under test rise time:

$$t^2_{observed} = t^2_{803} + t^2_{scope} + t^2_{c.u.t.}$$

or

$$t_{c.u.t.} = \sqrt{t^2_{observed} - t^2_{803} - t^2_{scope}}$$

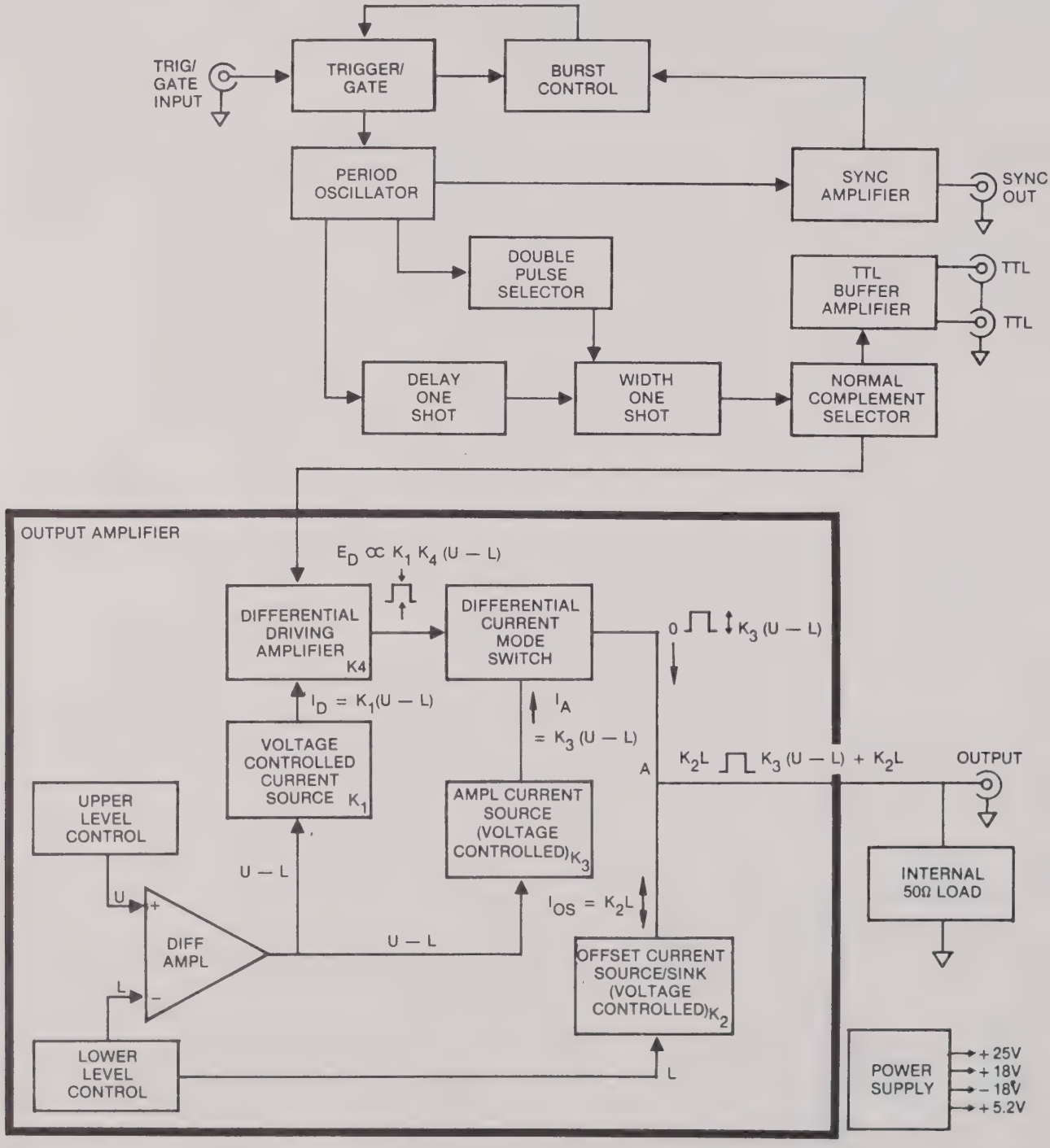


Figure 4-1. Overall Block Diagram

SECTION 4
CIRCUIT DESCRIPTION

4.1 OVERALL BLOCK DIAGRAM

The Model 803 is made up of ten major circuit blocks: trigger/gate, period oscillator, sync amplifier, burst control logic, double pulse selector, delay one shot, width one shot, normal complement selector, TTL buffer amplifier, output amplifier, and a power supply. (See figure 4-1.)

The circuitry is on two PC boards with a combination of TTL and ECL logic gates, and discrete semiconductor devices. The TTL and ECL logic, in addition to making up individual circuit blocks, serve as a signal coupling medium between the blocks. The signal path changes depending on the mode selected.

4.2 PERIOD OSCILLATOR

A simplified diagram of the period oscillator, an ECL multivibrator, appears in figure 4-2.

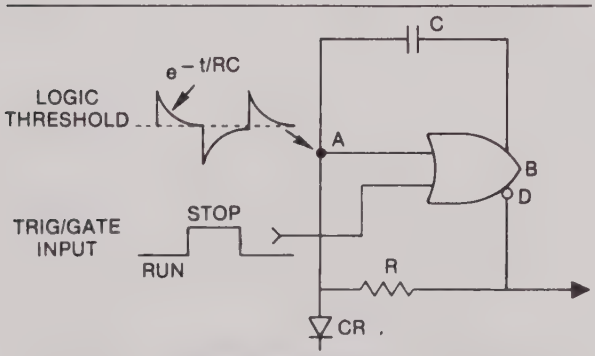


Figure 4-2. Simplified Diagram of the Period Oscillator

The RC time constant determines the charge and discharge rates for capacitor C and, therefore, the frequency of operation.

Positive feedback via the path through C results in a stable oscillator. Varying resistor R changes the frequency over a 10:1 range. Note that since the charging and discharging current are equal but opposite, the resulting waveform has a 50% duty cycle.

The oscillator may be gated via the trig/gate input. Whenever this input is high, it forces output D low and stops the oscillator. The oscillator starts synchronously when the input goes low.

For burst, the oscillator is enabled by a trigger and disabled by a command from the burst control logic.

4.3 TRIGGER/GATE

The trigger/gate circuit receives and processes external or manual triggers and, from the burst control logic and burst mode logic, commands to control the period oscillator for trigger, gate or burst operation. Triggering of the period oscillator occurs on the positive transition of the trigger/gate input signal or when the MAN TRIG switch is pressed.

The trigger/gate circuit, shown in figure 4-1 as a single block, is actually divided between the generator and burst boards.

Circuits located on the burst board consist of two steering gates and a manual trigger debounce circuit. The steering gates route the trigger pulses back to the trigger circuit on the generator board, or the burst control logic, depending on the mode selected. The manual trigger debounce circuit provides a positive transition, which enables the oscillator, each time the MAN TRIG switch is pressed.

On the generator board, the trigger circuit consists of an ECL gate connected to provide positive feedback which forms a Schmitt trigger. An input divider adjusts the input to approximately +1.4V, making the input compatible with the TTL signal from the burst board.

The output of the trigger/gate circuit is always connected to the period oscillator. If the control line to the oscillator is low, the oscillator will run continuously and if high, it will stop the oscillator.

When the trigger mode is selected, node A of the oscillator is pulled low via diode CR. The IC now acts as an inverter to the TRIG/GATE INPUT signal and passes the signal to the delay one-shot.

4.4 BURST CONTROL CIRCUIT

The burst control circuit (ref: figures 4-1 and 4-3) allows the oscillator to generate a precise number of pulses for each trigger input received. To do this, six TTL circuits (one shot, burst clock logic, counter load latch, five digit BCD up counter, five digit BCD switches, and burst terminate decoder) on the burst board are interconnected with the sync amplifier

(oscillator input to the burst circuit) on the generator board and the trigger circuit on the burst board.

To best understand the operation of the burst control circuit refer to the expanded block diagram figure 4-3 and the following explanation.

To initiate a burst, a trigger must be applied to the instrument. A trigger does two things: first, it provides a direct clear to all five counters; second, it provides a TTL low to the input of the counter load latch. The direct clear forces the counter outputs to TTL lows; this forces the burst terminate decoder logic to a TTL high which enables the oscillator. Once the oscillator begins operation, the pulse is routed through the burst clock logic to the counter's clock input and the counter load latch. The oscillator's pulses clock the counter load latch which, in turn, loads the data into the counters. The data loaded into the counters are the nines' complement of the digits selected by the five digit BCD switch: this corresponds to the desired burst length. Next, each successive clock pulse will increase the counters by one count until the counter reaches the terminal count (a BCD nine in the four most significant counters and a BCD eight in the least significant counter). At terminal count the burst terminate decode logic output to a TTL low, thus disabling the oscillator.

Because one oscillator pulse is generated before the counters begin the count, the last pulse must be subtracted from the pulse count. To do this, the least significant bit from least significant counter is ignored by the decoder logic; thus making the counter effectively a BURST -1 counter while the instrument produces a full burst count.

4.5 SYNC AMPLIFIER

The sync amplifier acts as a buffer amplifier between the oscillator and the SYNC OUT BNC. It provides a TTL output level from a 50Ω source. The output from the sync circuit is an approximate square wave at the oscillator frequency.

A separate output from the sync amplifier provides the clock input to the burst control logic circuit.

When gating the generator, the sync signal should be taken from the gating source rather than the 803.

4.6 DELAY ONE SHOT

The delay one shot allows an adjustable time between the sync output and the leading edge of the final output pulse. The delay one shot consists of an ECL gate and discrete circuit one shot multivibrator. When the delay circuit is triggered by the oscillator, a timing capacitor is discharged by a constant current source until a threshold point is reached. The circuit then resets by rapidly recharging the timing capacitor. The output pulse from the ECL gate has a width proportional to the timing capacitor value and the magnitude of the current source. The pulse width is independent of the triggering rate as long as it is less than 70% of the trigger period.

4.7 WIDTH ONE SHOT

The width one shot determines the width of the output pulse. The width one shot, triggered by the trailing edge of the delay one shot, is identical in operation to the delay one shot. In the double pulse mode it is triggered on the leading and trailing edges of the delay one shot pulse. When the mode is selected, the delay and width one shots are disabled and the oscillator square wave passes through them to the output amplifier. An exclusive OR gate allows either phase of the width one shot output to be selected as the signal to drive the output amplifier.

4.8 DOUBLE PULSE SELECTOR

The double pulse selector routes a pulse coincident with the leading edge of the oscillator to the width one shot. This pulse together with a delayed pulse will trigger the width one shot. The selector consist of an ECL gate and the DOUBLE PULSE switch. For double pulse timing, see figure 4-9.

4.9 TTL BUFFER AMPLIFIER

The output of the width one shot drives a current mode switch, the TTL buffer amplifier, in addition to the output amplifier. This switch is designed to drive TTL level signals into 50Ω loads. Both signal phases, TTL and $\overline{\text{TTL}}$, are available simultaneously.

4.10 NORMAL/COMPLEMENT SELECTOR

The normal/complement selector determines the phase of the output pulse relative to the sync output. The selector consists of three ECL Exclusive OR/NOR gates and the COMP switch.

4.11 OUTPUT AMPLIFIER

The output amplifier (figure 4-1) establishes the pulse lower level by passing a constant current through the 50Ω load. The current is provided by a voltage controlled current source programmed by the lower level control potentiometer. A current pulse of the proper amplitude is now added at node A to this base line for the duration of the width one shot time. The amplitude of the current pulse is equal to the difference between the upper and lower level controls (U — L). The upper level will be (U — L) + L = U at the output.

In order to generate a current pulse, the width one shot drives a current mode switch via a driving amplifier. The current mode switch connects a current source to the load whenever the output of the width one shot is high. The current source is voltage controlled and its output is equal to the difference between the upper and lower level controls (U - L).

The output of the driving amplifier varies in amplitude directly with the output level programmed by the level controls. This prevents overdriving the current mode switch and distorting the output at low levels.

Note that changing the lower level control will change both the base line and the current pulse amplitude which will cause the upper level to remain fixed. That is (U — L) + L = U, regardless of the value of L.

The internal 50Ω load may be switched in or out depending on the application.

4.12 POWER SUPPLY

The power supply converts the line voltage to four regulated dc voltages which power all the other circuit blocks.

4.13 MODES OF OPERATION

The major circuit block connections depend on the mode of operation selected. Block diagrams of the major modes and key waveforms are shown in figures 4-4 through 4-10.

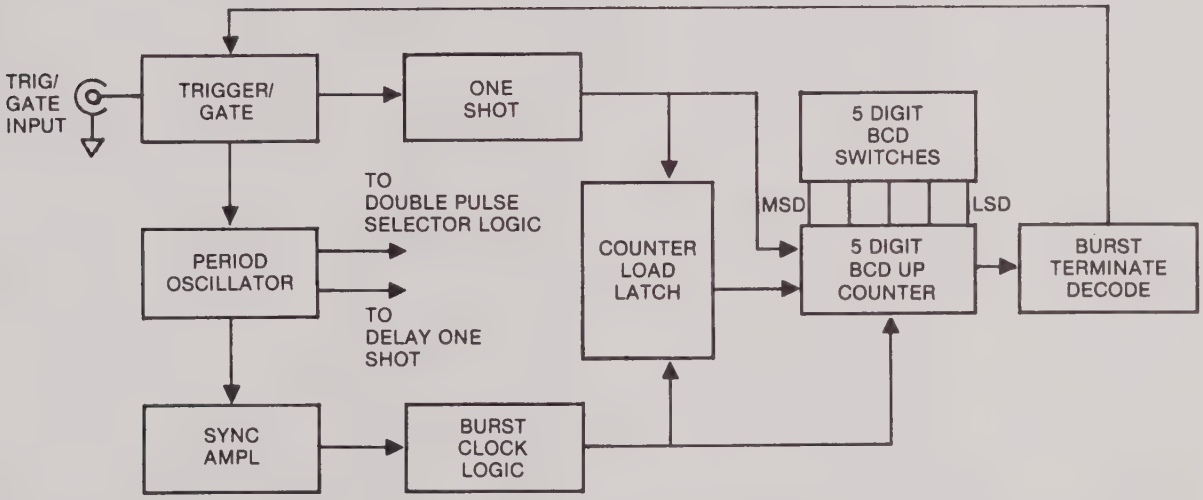


Figure 4-3. Burst Control Block Diagram

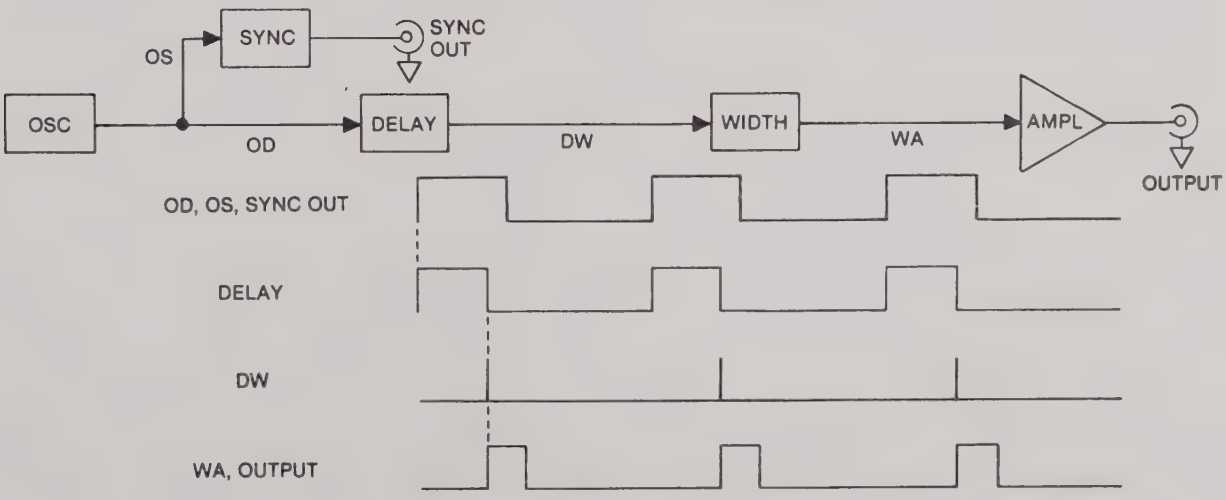


Figure 4-4. Continuous Mode

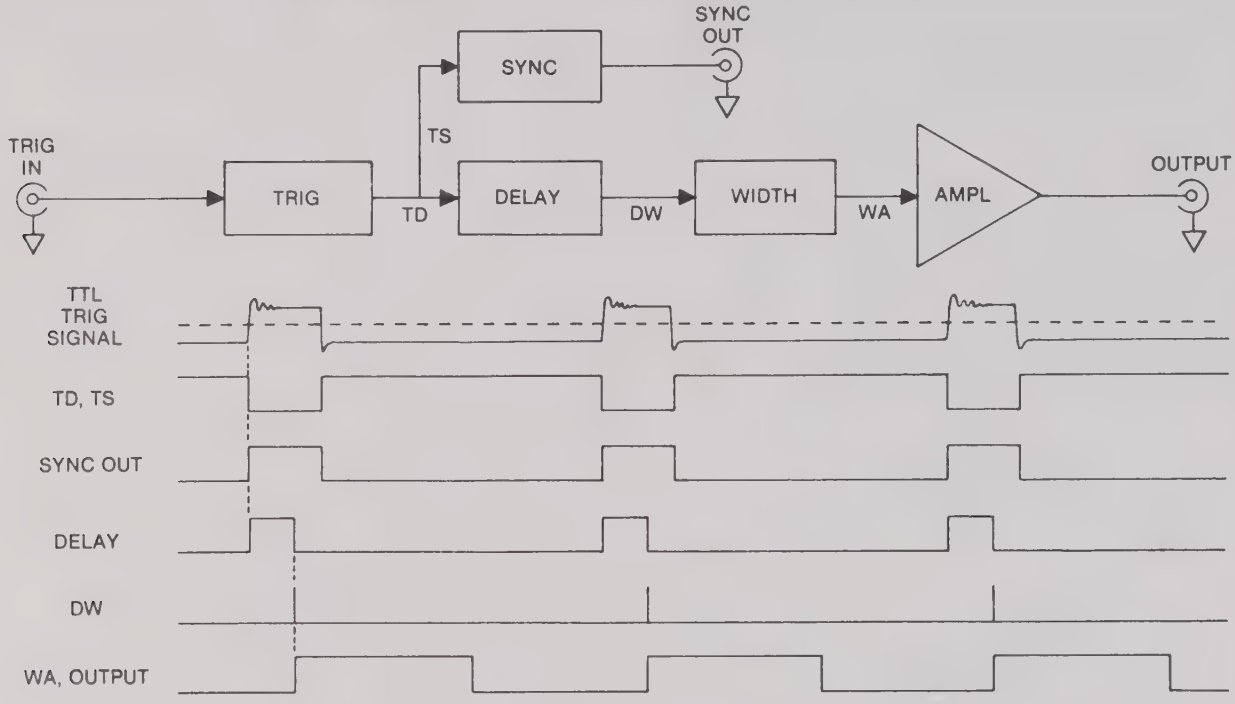


Figure 4-5. Trigger Mode

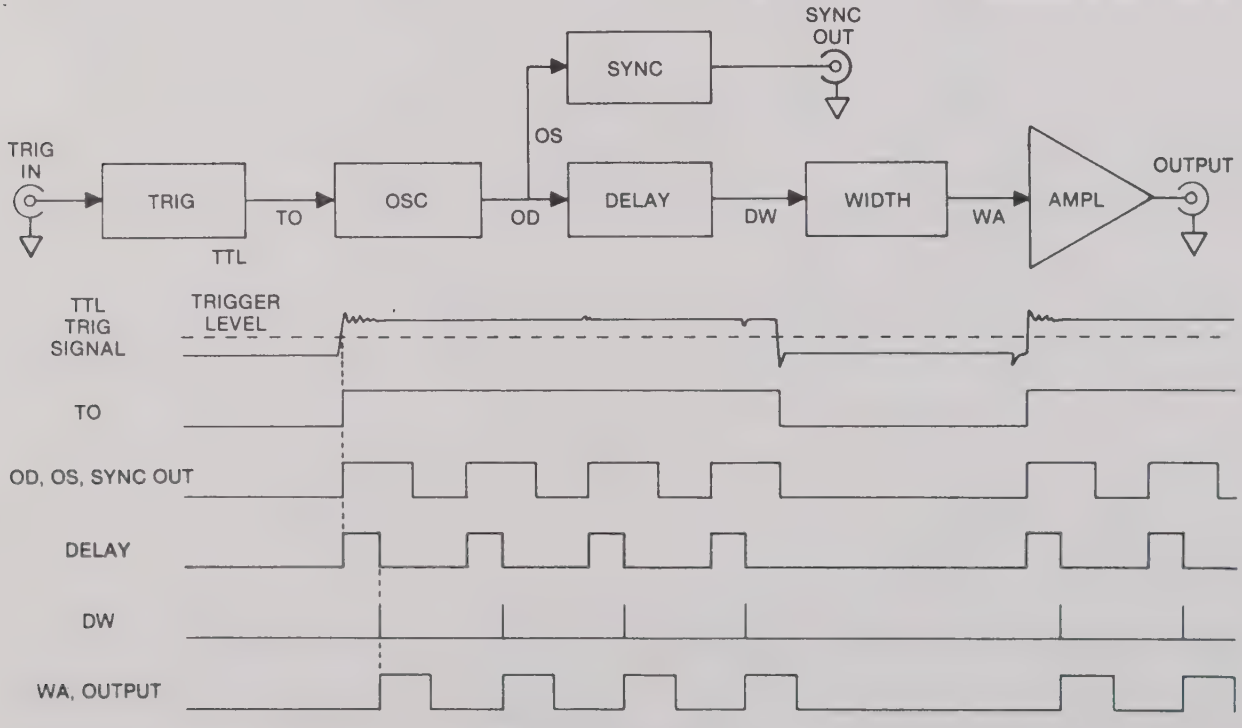


Figure 4-6. Gate Mode

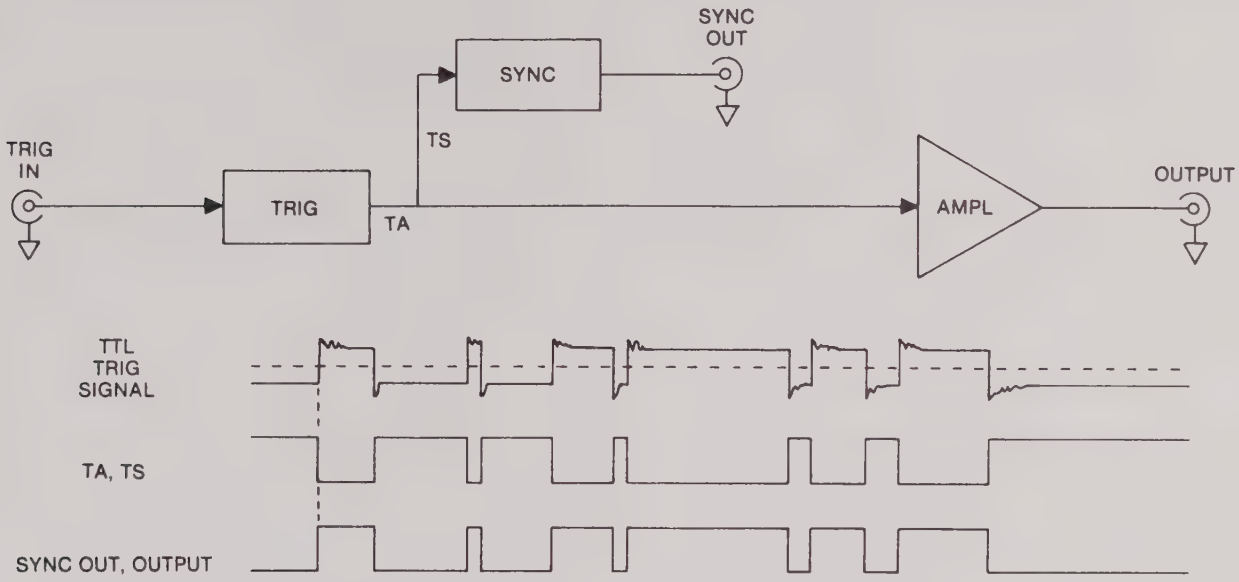


Figure 4-7. External Width Mode

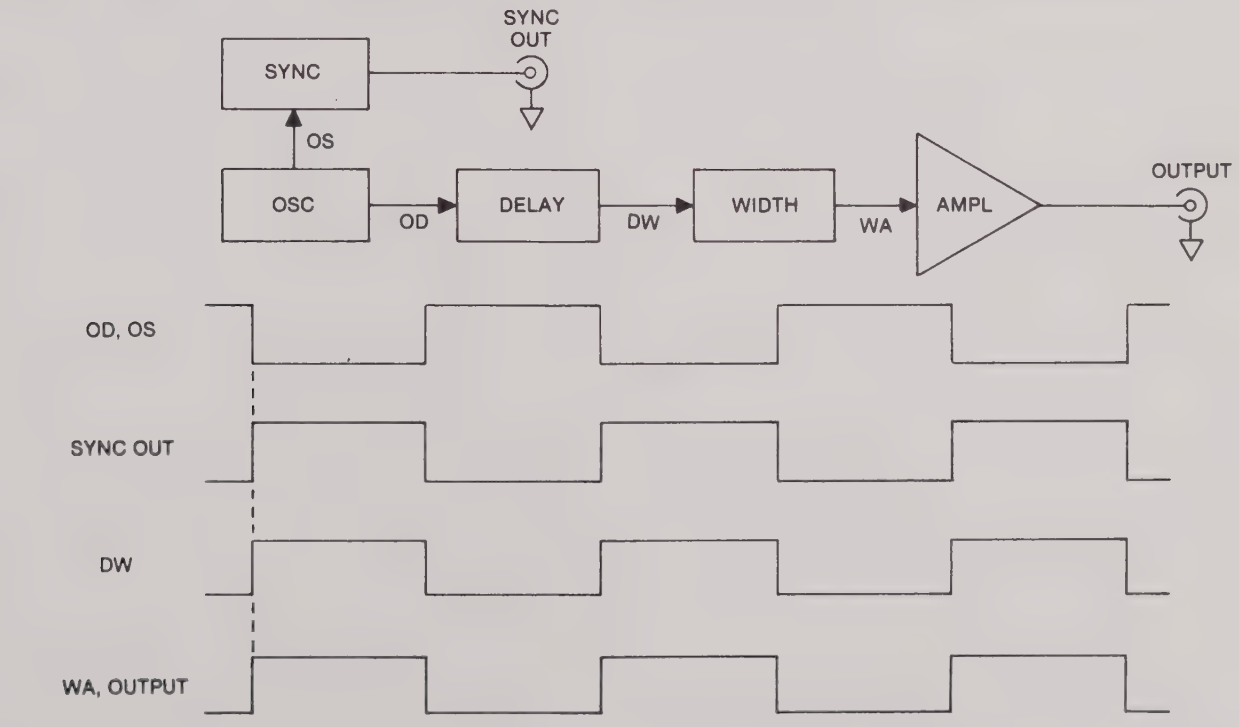


Figure 4-8. Continuous Square Wave Mode

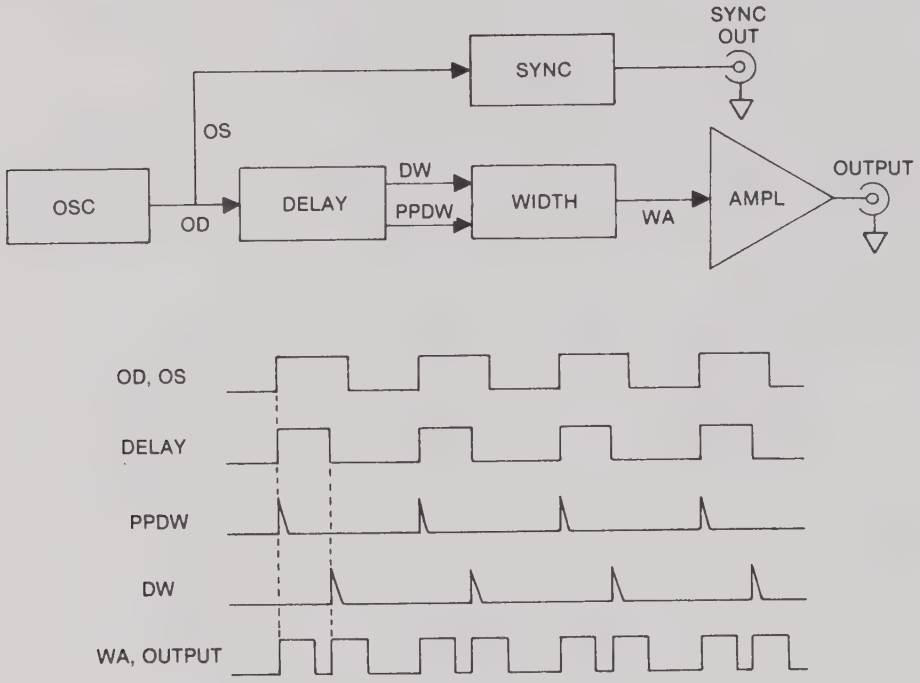


Figure 4-9. Continuous Double Pulse Mode

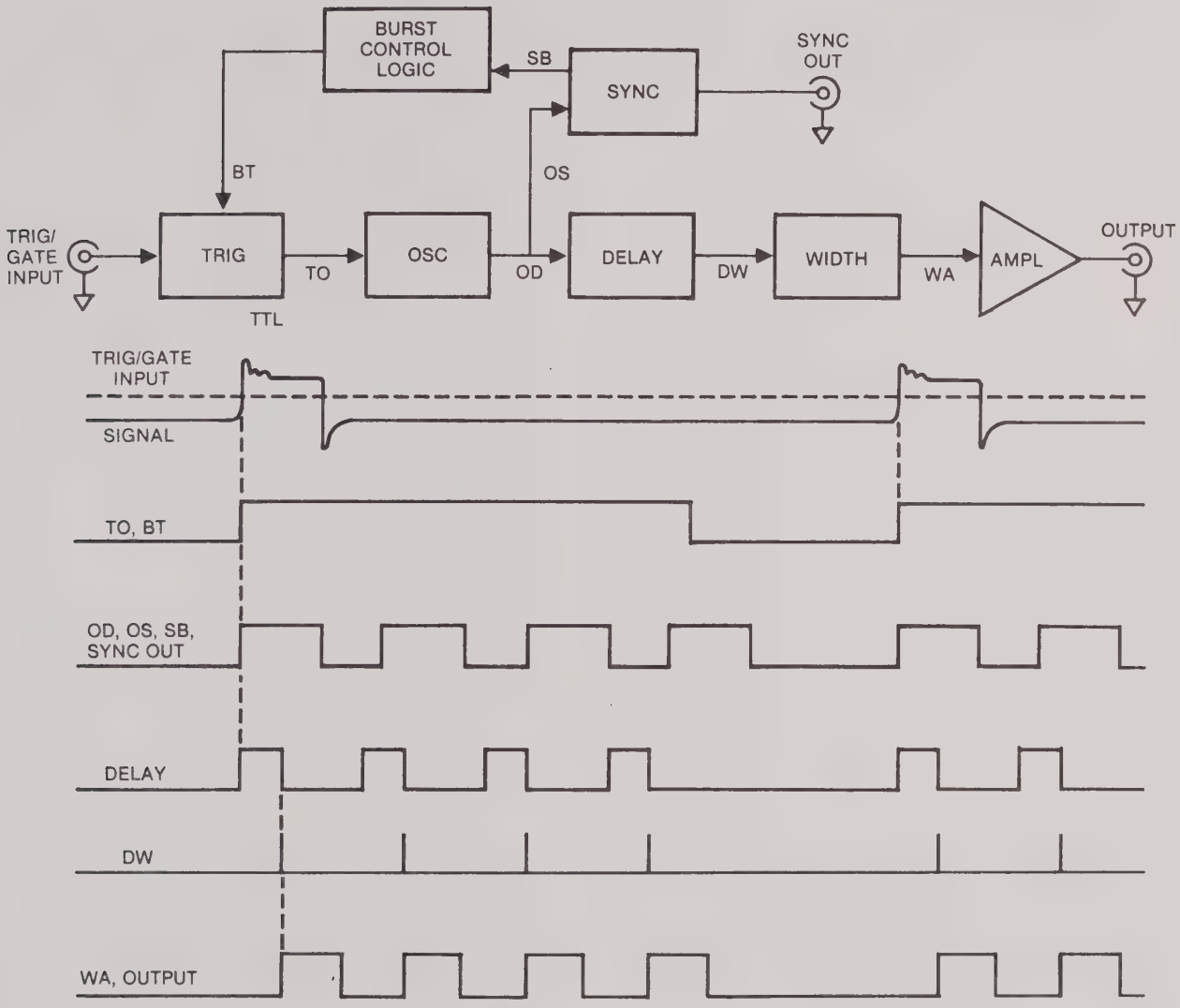


Figure 4-10. Triggered Burst Mode

SECTION 5
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

5.2 REQUIRED TEST EQUIPMENT

Voltmeter	Millivolt dc measurement (0.1% accuracy)
Oscilloscope, Dual Channel	500 MHz bandwidth
Oscilloscope, Sampling	1 GHz bandwidth
Counter	55.0 MHz (0.01% accuracy) with totalization capability
50Ω Feed thru	±0.1% accuracy, 2W (3 ea)
10 × 50Ω Feedthru Attenuator	±0.1% accuracy, 2W
Function Generator	5 kHz, TTL square wave
RG58U Coax Cable	3 ft length BNC male contacts
BNC Tee	1 male, 2 female connectors

5.3 REMOVING GENERATOR COVERS

1. Invert the instrument and remove the four screws in the cover.
2. Turn the instrument upright, remove the top cover, and remove the four screws securing the bottom cover.
3. Replace the cover and turn the instrument upside down.

NOTE

Remove the cover only when it is necessary to make adjustments or measurements.

5.4 CALIBRATION

After referring to the following preliminary data, perform calibration, as necessary, per table 5-1. If performing partial calibration, check previous settings and adjustments for applicability. See figure 5-1 for calibration point location.

1. Unless otherwise noted, all measurements made at the TTL, TTL or OUTPUT connectors must be terminated into a 50Ω (±0.1%) load.
2. Start the calibration by connecting the unit to an ac source and setting these front panel switches as follows:

PERIOD	200 ns / 2μs
PERIOD VERNIER	Full cw
PULSE MODE	OFF
DELAY	OFF
WIDTH	⎍
LOWER LEVEL	−10V
UPPER LEVEL	+10V
BURST/CONT/GATE	Gate

3. Allow the unit to warm up at least 30 minutes for final calibration. Keep the instrument covers on to maintain heat. Remove covers only to make adjustments or measurements.

Table 5-1. Calibration Chart

Step	Check	Tester	Cal Points	Control Settings	Adjust	Desired Results	Remarks
1	Power Supply	DVM	—	—	R1	+25V ±0.10V	
2			—	—	R7	+18V ±0.05V	
3			—	—	R2	−18V ±0.05V	
4			—	—	R3	+5.2V ±0.05V	

Table 5-1. Calibration Chart (Continued)

Step	Check	Tester	Cal Points	Control Settings	Adjust	Desired Results	Remarks
5	Duty Cycle	Scope	TTL	R157: Full cw	R18	50% duty cycle ±0.5%	
6				PERIOD: 20 ns / 200 ms PERIOD VERNIER: Full ccw	C27	51 MHz (19.6 ns)	
7	Output Amplifier	DVM	OUTPUT	PERIOD: TRIG COMP: ON LOWER LEVEL: Full cw, then full ccw	R101	Equal cw & ccw voltage	
8				LOWER LEVEL: Full cw	R97	+10.5V ±0.05V	Repeat steps 7 and 8 once.
9				LOWER LEVEL: 0V on DVM			Loosen and re-align LOWER LEVEL knob at 0V, if necessary.
10				UPPER LEVEL: Full cw COMP: OFF	R107	+10.5V ±0.05V	
11				UPPER LEVEL: 0V on DVM			Loosen and re-align UPPER LEVEL knob at 0V, if necessary. Make sure mechanical interlock on knob is engaged.
12			TP1	UPPER LEVEL: Full cw	R110	−0.6V ±0.05V	
13	Overshoot & Ringing	Scope	OUTPUT	INT 50Ω: ON LOWER LEVEL: 0V	R124 C56	Minimum overshoot & ringing	
14				UPPER LEVEL: +0.5V	R133	Minimum ringing	Repeat steps 13 and 14 once.
15	Overshoot & Rise Time			UPPER LEVEL: Full cw LOWER LEVEL: Make a +5V pulse	R157	Minimum overshoot	Maintain ≥5.1V pulse and ≤5 ns rise time. A slight readjustment of R110 may be necessary.

SECTION 6
TROUBLESHOOTING

6.1 INTRODUCTION

This section is organized as follows:

Safety
Circuit Board Access
Basic Techniques
Troubleshooting Individual Components
Flow Charts

Refer to paragraph 5.2 for required test equipment.

NOTE

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 SAFETY

6.2.1 Precautions

Refer all servicing and calibration to a qualified electronic technician.

Always disconnect the power cord when working on this instrument, unless electrical measurements are being taken: Never attempt to isolate the safety ground lug of the power cord.

Be sure that the fuse rating is correct and that the line voltage selector card is set to the proper range (refer to section 2).

Line voltage is present on the circuit board of the ac power connector, *even when the power switch is off.* This voltage is only accessible if the shield is removed from the ac power connector.

6.2.2 Safety Check

Disconnect the power cord from facility power and check that the resistance from the cord earth ground terminal to the instrument front panel metal is less than one ohm. Press the power switch on and measure the resistance between the instrument front panel metal and each of the power cord's two matching terminals. Resistance to each terminal should be greater than two megohms. Check the fuse for proper type and value. Remove the instrument covers and inspect the power supply and circuit boards for evidence of overheating or arcing. Check lines and cables for good physical connections. Correct any discrepancies detected.

6.3 CIRCUIT BOARD ACCESS

Remove the top cover (paragraph 5.3) for access to the circuit boards. To remove the burst board, remove the four screws securing the burst board. Remove the four screws securing the board to the bottom cover for access to the bottom of the board.

6.4 BASIC TECHNIQUES

Troubleshooting requires no special technique. Listed below are a few reminders of basic electronic fault isolation.

1. Check control settings carefully. Many times a seemingly malfunction is an incorrect control setting, or a knob that has loosened on its shaft.
2. Check associated equipment connections. Make sure that all connections are securely connected to the correct connector.
3. Perform the calibration procedure. Many out-of-specification indications can be corrected by performing specific calibration procedures.
4. Visually check the interior of the instrument. Look for such indications as broken wires, charred components and loose leads.
5. Try to isolate the problem to a specific circuit by checking generator operation in all modes and referring to the block diagrams for each mode (see figures 4-4 thru 4-10). After the problem has been isolated to a specific stage, check the dc operating voltages at the pins of all solid state devices within that stage.
6. Check the associated passive elements with a high impedance ohmmeter (instrument unplugged) before replacing a suspected semiconductor device.

6.5 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.5.1 Transistor

A transistor is defective if more than one volt is measured across its base emitter junction in the forward direction.

A transistor when used as a switch may have a few volts reverse bias voltage base to emitter.

If the collector and emitter voltages are the same, but the base emitter voltage is less than 500 mV forward voltage (or reversed bias), the transistor is defective.

A transistor is defective if its base current is larger than 10% of its emitter current (calculate currents from voltage across the base and emitter series resistors).

6.5.2 Diode

A diode is defective if there is greater than 1 volt (typically 0.7 volts) forward voltage across it (except Zener and LED).

6.5.3 Operational Amplifier

The "+" and "−" inputs of an operational amplifier will have less than 15 mV voltage difference when operating under normal conditions.

If the output voltage stays at maximum positive, "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.5.4 FET Transistor

No gate current should be drawn by the gate of an FET transistor. If so, the transistor is defective.

The gate-to-source voltage is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for 2N5485, and the source voltage is more negative than gate voltage for a 2N5462. Otherwise, the FET is defective.

6.5.5 MOSFET Transistor

For MOSFET's such as the SD214 or SD215, a positive gate source voltage causes the device to conduct drain current. Zero volts or a negative voltage cause the device to pinch off. A MOSFET transistor can be damaged by a static charge buildup when out of the circuit. Keep MOSFET leads shorted together until soldered in the circuit board.

6.5.6 Capacitor

Shorted capacitors have zero volts across their terminals.

An unopened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.

6.5.7 ECL Gate

The emitter coupled logic using NOR logic is:

Inputs		NOR Output	Exclusive OR Output
A	B	$C = A + B$	$C = \overline{A \oplus B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	1

The levels are:

"0" = +3.4V ±0.1V
"1" = +4.3V ±0.1V

Never short the output of an ECL gate to ground; this will damage the output transistor in the gate. Any input may be pulled high, even when driven by an output of another gate, by connecting a diode between the input and the +5.2V supply (anode to supply).

6.5.8 TTL Gate

The device is operating correctly if the output high state is > +2.4V and low state is < +0.5V.

The input must show the same two levels as described above. If the levels are between +0.8V and +2.0V, the connection to the driving circuit output is open.

6.6 FLOW CHARTS

The flow charts (see figures 6-1 thru 6-6) help isolate any malfunction to a specific stage. If you already know the specific circuit block at fault, go directly to that block in the flow chart. If a problem cannot be isolated to a portion of a flow chart, then follow the flow chart from the beginning.

If the problem cannot be located, return the instrument to the factory for servicing, with a description of the failure.

Before performing flow chart troubleshooting, set the front panel controls as follows:

PERIOD ..... 2μs / 20μs
PERIOD VERNIER ..... 12 o'clock
DELAY ..... 10 ns / 100 ns
DELAY VERNIER ..... 12 o'clock

WIDTH	100 ns / 1μs
WIDTH VERNIER	12:00
LOWER LEVEL	−10V
UPPER LEVEL	+10V
DBL PULSE	OFF
COMP	OFF
INT 50Ω	ON
BURST	00004
BURST/CONT/GATE	CONT

Connect both the sync and the output BNC's to an oscilloscope with 3 foot 50Ω cables terminated with 50Ω feedthroughs.

When troubleshooting the output amplifier, the flow chart in figure 6-6 should be followed. In addition, tables 6-1 and 6-2 provide additional guidance as to what voltages exist at the semiconductor devices and how they should vary with the output level controls.

Table 6-1. Level Control Dependent Voltages

Level Control Knob Setting	Output Waveform Into 50Ω	E17 Voltage Upper Level	E16 Voltage Lower Level	TP1	IC7-6	Emitter of Q6	Emitter of Q19
	+10	−18	−18	−18	−3.6	+8.1	+22
	+10 0	−18	0	−0.6	0	+8.1	+22
	+ 5 − 5	−9	+9	−0.6	+1.8	+8.1	+22
	0	0	0	−18	0	0	+25
	0 −10	0	+18	−0.6	+3.6	+8.1	+22
	−10	+18	+18	0	+3.6	0	+25

Table 6-2. Transistor Voltages

NOTE

These voltages apply with the controls set as follows.

PERIOD ..... *TRIG*
DELAY ..... *OFF*
WIDTH ..... ⎍
COMP ..... *OFF*
DBL PULSE ..... *OFF*
INT 50Ω ..... *ON*
UPPER LEVEL ..... *Max cw*
LOWER LEVEL *0V*

Transistor	B	C	E	Transistor	B	C	E
Q6	+8.7	+20.8	+8.1	Q22	+18.6	+12	+20.5
Q7	−0.6	−0.6	0	Q23	+10.8	0	+11.4
Q8	0	+18	≈0	Q24	+11.4	0	+12.0
Q9	0	−18	≈0	Q25	+12.0	+10.0	+12.6
Q10	+18	+13	+18	Q26	+15.2	+13.0	+15.8
Q11	−18	−13	−18	Q27	+12.0	+10.0	+12.6
Q12	−0.6	+0.3	−1.2	Q28	+15.2	+13.0	+15.8
Q16	+4.3	+6.4	+3.7	Q29	+12.0	+10.0	+12.6
Q17	+3.4	+9.8	+3.7	Q30	+14.6	+12.0	+15.2
Q18	+20.8	21.4	+21.4	Q31	−12.0	+10.0	−12.6
Q19	+21.4	21.4	+22.0	Q32	−12.0	+10.0	−12.6
Q21	+18.6	+12	+20.5	Q35	+18.0	+12.0	+18.6

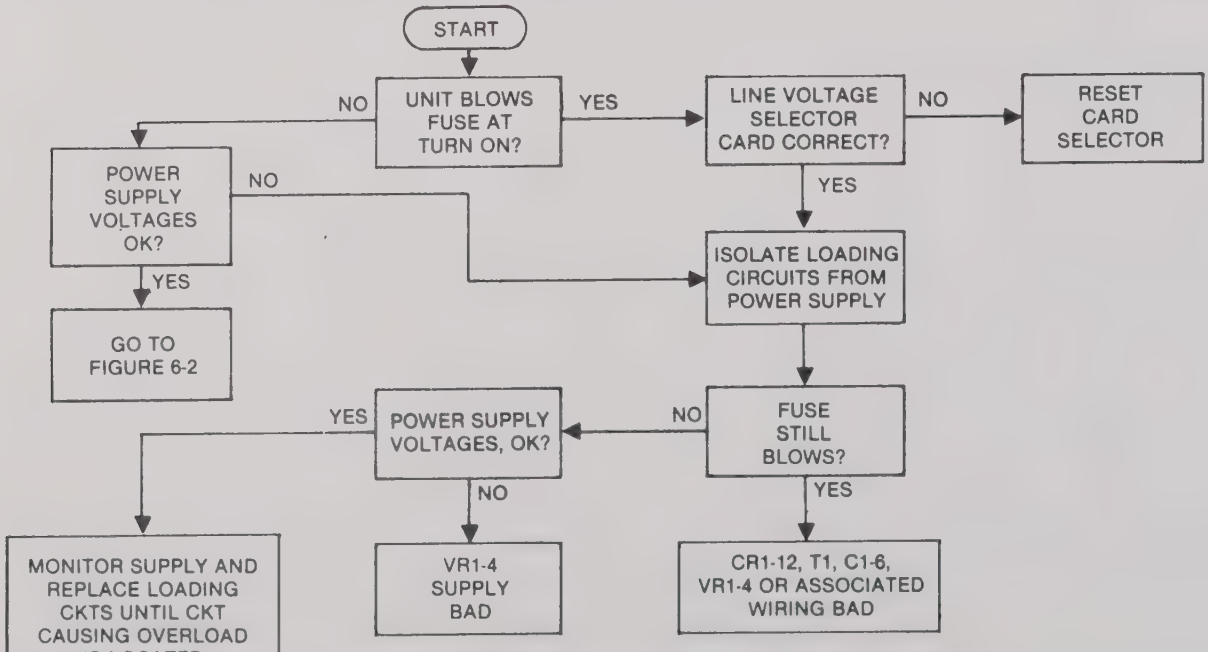


Figure 6-1. Power Supply Troubleshooting

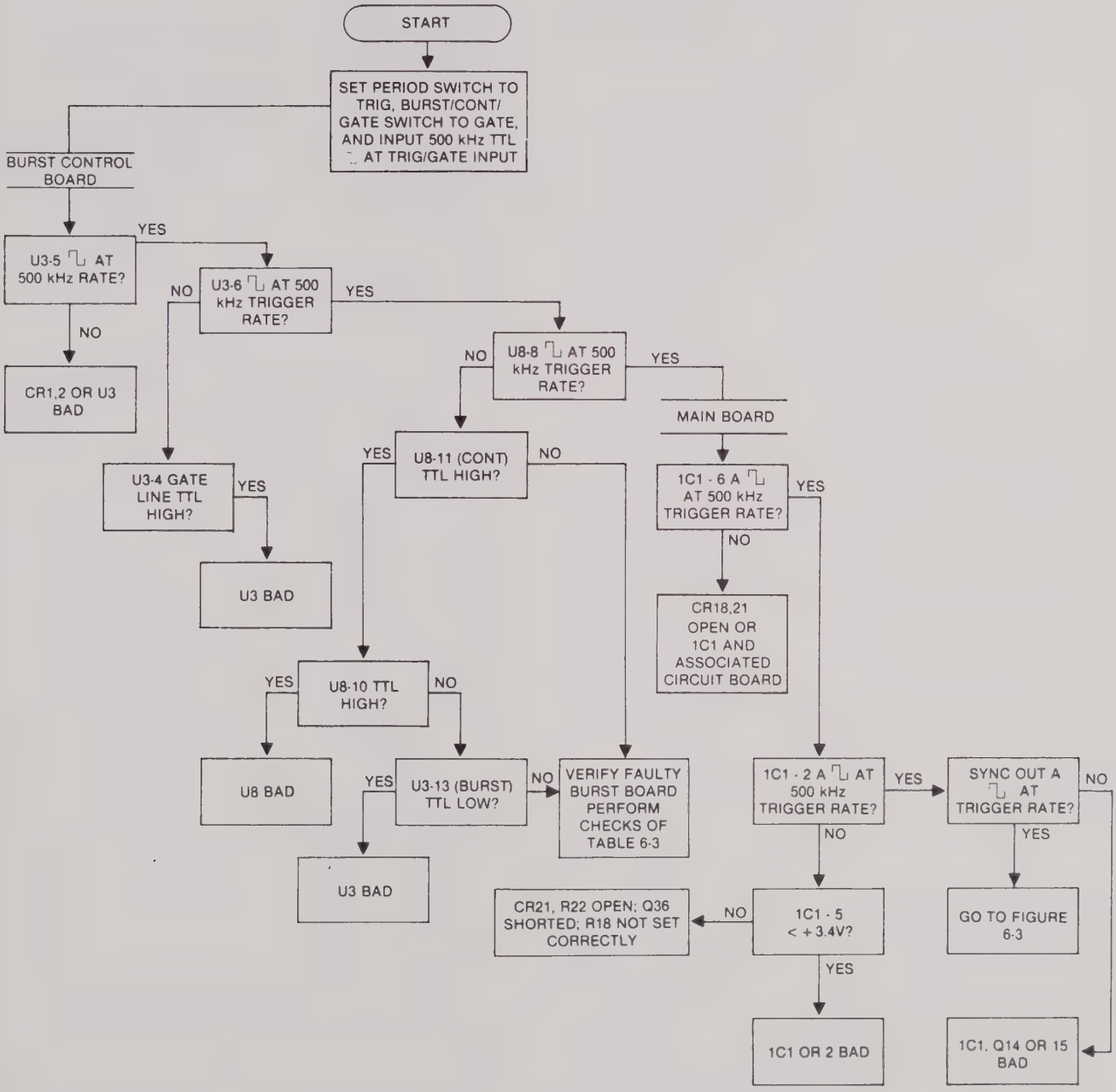


Figure 6-2. Trigger Circuit Troubleshooting

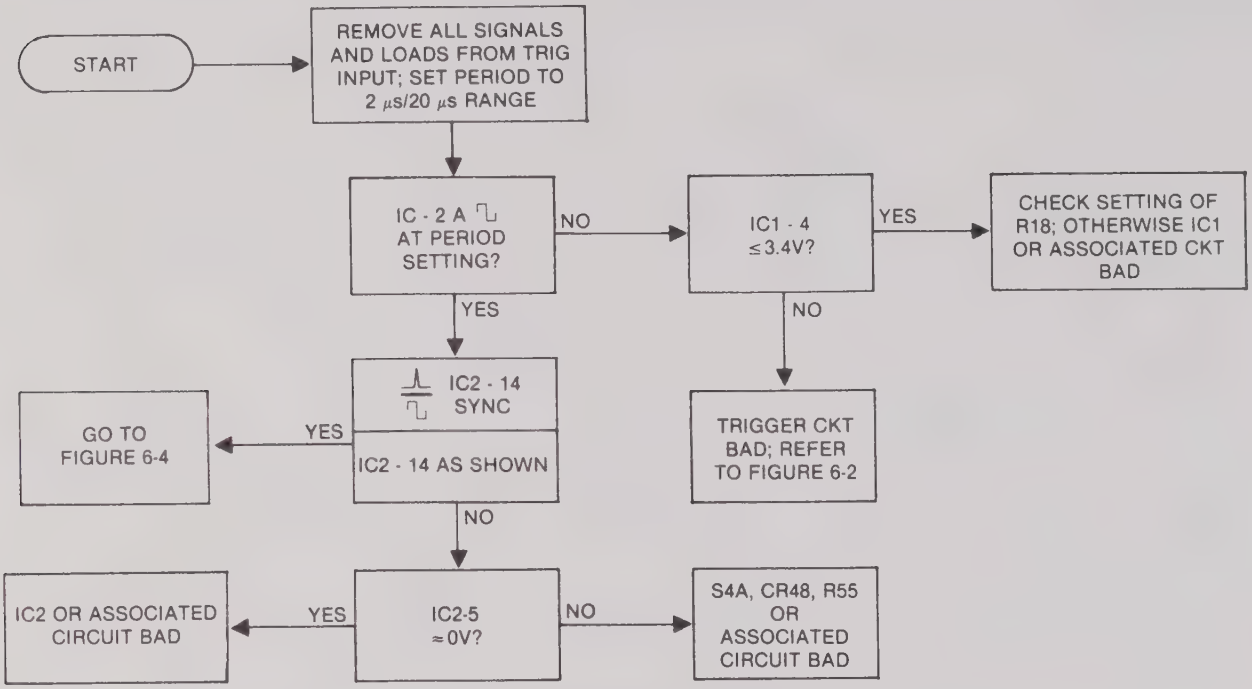

START
REMOVE ALL SIGNALS AND LOADS FROM TRIG INPUT; SET PERIOD TO 2 μs/20 μs RANGE
IC - 2 A AT PERIOD SETTING?
NO
IC1 - 4 ≤3.4V?
YES
CHECK SETTING OF R18; OTHERWISE IC1 OR ASSOCIATED CKT BAD
YES
NO
IC2 - 14 SYNC
IC2 - 14 AS SHOWN
YES
GO TO FIGURE 6-4
TRIGGER CKT BAD; REFER TO FIGURE 6-2
NO
IC2 OR ASSOCIATED CIRCUIT BAD
YES
IC2-5 ≈0V?
NO
S4A, CR48, R55 OR ASSOCIATED CIRCUIT BAD

Figure 6-3. Oscillator Troubleshooting

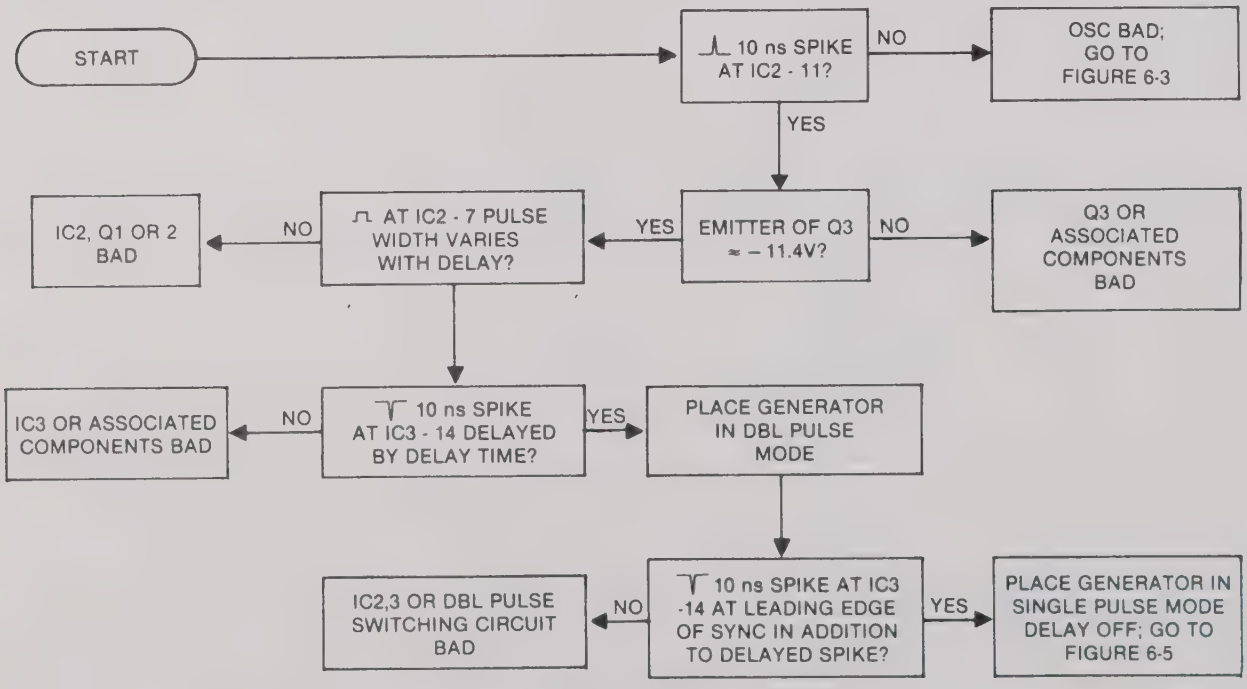

START
10 ns SPIKE AT IC2 - 11?
NO
OSC BAD; GO TO FIGURE 6-3
YES
EMITTER OF Q3 ≈ −11.4V?
YES
NO
Q3 OR ASSOCIATED COMPONENTS BAD
AT IC2 - 7 PULSE WIDTH VARIES WITH DELAY?
NO
IC2, Q1 OR 2 BAD
10 ns SPIKE AT IC3 - 14 DELAYED BY DELAY TIME?
NO
IC3 OR ASSOCIATED COMPONENTS BAD
YES
PLACE GENERATOR IN DBL PULSE MODE
10 ns SPIKE AT IC3 -14 AT LEADING EDGE OF SYNC IN ADDITION TO DELAYED SPIKE?
NO
IC2,3 OR DBL PULSE SWITCHING CIRCUIT BAD
YES
PLACE GENERATOR IN SINGLE PULSE MODE DELAY OFF; GO TO FIGURE 6-5

Figure 6-4. Delay Circuit Troubleshooting

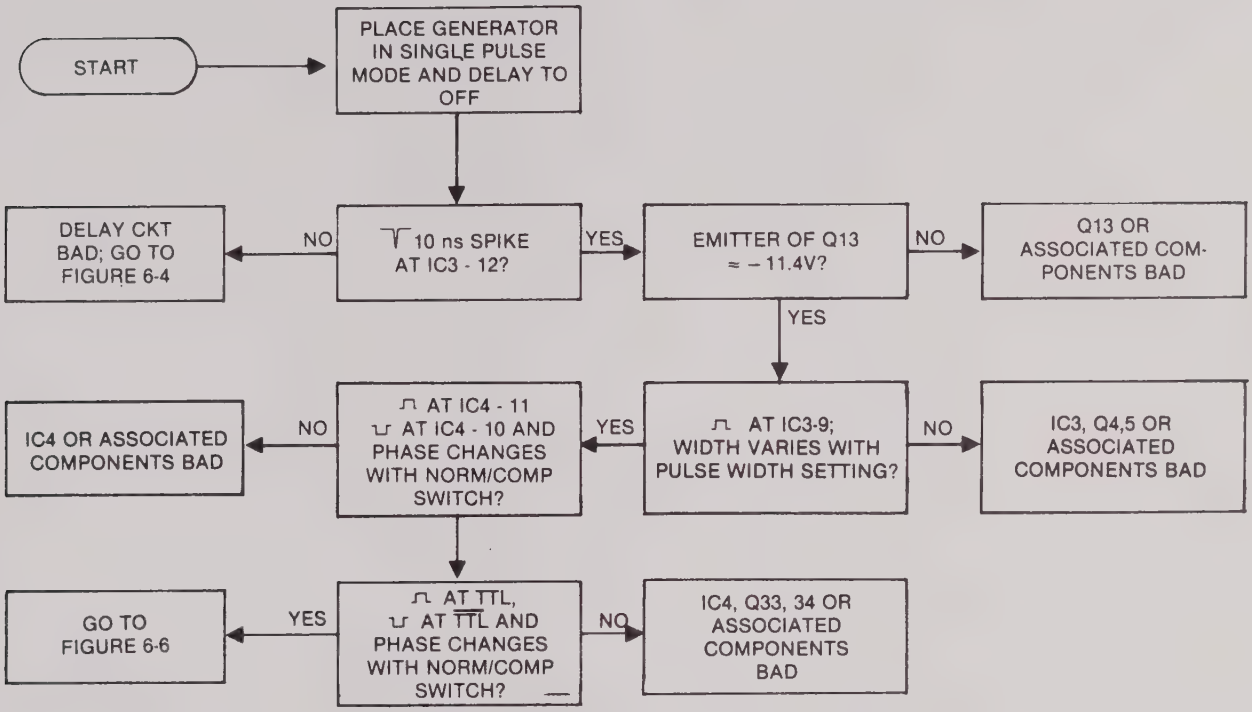

START
PLACE GENERATOR IN SINGLE PULSE MODE AND DELAY TO OFF
DELAY CKT BAD; GO TO FIGURE 6-4
NO
10 ns SPIKE AT IC3 - 12?
YES
EMITTER OF Q13 ≈ −11.4V?
NO
Q13 OR ASSOCIATED COMPONENTS BAD
YES
IC4 OR ASSOCIATED COMPONENTS BAD
NO
AT IC4 - 11
AT IC4 - 10 AND PHASE CHANGES WITH NORM/COMP SWITCH?
YES
AT IC3-9; WIDTH VARIES WITH PULSE WIDTH SETTING?
NO
IC3, Q4,5 OR ASSOCIATED COMPONENTS BAD
GO TO FIGURE 6-6
YES
AT TTL,
AT $\overline{\text{TTL}}$ AND PHASE CHANGES WITH NORM/COMP SWITCH?
NO
IC4, Q33, 34 OR ASSOCIATED COMPONENTS BAD

Figure 6-5. Width Circuit Troubleshooting

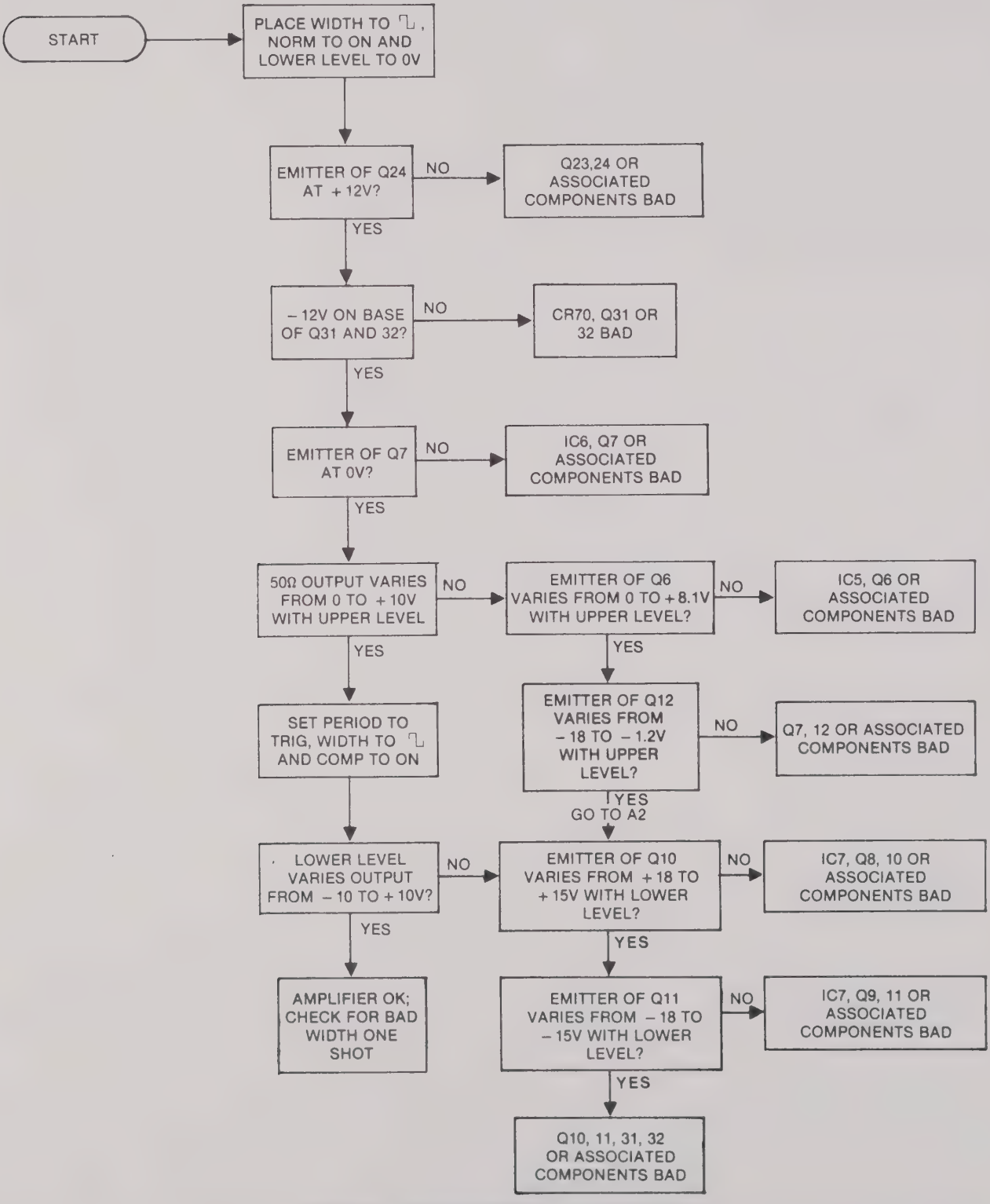

START
PLACE WIDTH TO ⎍, NORM TO ON AND LOWER LEVEL TO 0V
EMITTER OF Q24 AT +12V?
NO
Q23,24 OR ASSOCIATED COMPONENTS BAD
YES
–12V ON BASE OF Q31 AND 32?
NO
CR70, Q31 OR 32 BAD
YES
EMITTER OF Q7 AT 0V?
NO
IC6, Q7 OR ASSOCIATED COMPONENTS BAD
YES
50Ω OUTPUT VARIES FROM 0 TO +10V WITH UPPER LEVEL
NO
EMITTER OF Q6 VARIES FROM 0 TO +8.1V WITH UPPER LEVEL?
NO
IC5, Q6 OR ASSOCIATED COMPONENTS BAD
YES
YES
SET PERIOD TO TRIG, WIDTH TO ⎍ AND COMP TO ON
EMITTER OF Q12 VARIES FROM –18 TO –1.2V WITH UPPER LEVEL?
NO
Q7, 12 OR ASSOCIATED COMPONENTS BAD
YES
GO TO A2
LOWER LEVEL VARIES OUTPUT FROM –10 TO +10V?
NO
EMITTER OF Q10 VARIES FROM +18 TO +15V WITH LOWER LEVEL?
NO
IC7, Q8, 10 OR ASSOCIATED COMPONENTS BAD
YES
YES
AMPLIFIER OK; CHECK FOR BAD WIDTH ONE SHOT
EMITTER OF Q11 VARIES FROM –18 TO –15V WITH LOWER LEVEL?
NO
IC7, Q9, 11 OR ASSOCIATED COMPONENTS BAD
YES
Q10, 11, 31, 32 OR ASSOCIATED COMPONENTS BAD

Figure 6-6. Output Amplifier Troubleshooting

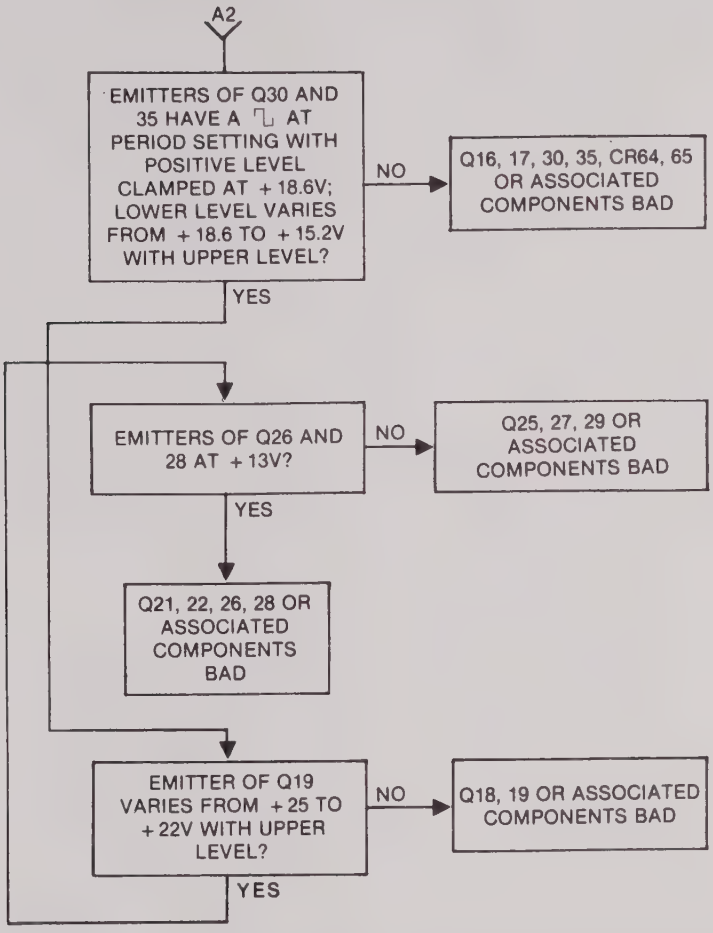

A2
EMITTERS OF Q30 AND 35 HAVE A ⎍ AT PERIOD SETTING WITH POSITIVE LEVEL CLAMPED AT +18.6V; LOWER LEVEL VARIES FROM +18.6 TO +15.2V WITH UPPER LEVEL?
NO
Q16, 17, 30, 35, CR64, 65 OR ASSOCIATED COMPONENTS BAD
YES
EMITTERS OF Q26 AND 28 AT +13V?
NO
Q25, 27, 29 OR ASSOCIATED COMPONENTS BAD
YES
Q21, 22, 26, 28 OR ASSOCIATED COMPONENTS BAD
EMITTER OF Q19 VARIES FROM +25 TO +22V WITH UPPER LEVEL?
NO
Q18, 19 OR ASSOCIATED COMPONENTS BAD
YES

Figure 6-6. Output Amplifier Troubleshooting (Continued)

Table 6-3. Burst Board Verification

Step	Check	Tester	Control Settings	Desired Results
1	Generator	Scope. Horizontal: 5μs/div, Vertical: 2V/div.	PERIOD: 2μs / 20μs. DELAY: OFF. WIDTH: ⎍ PULSE MODE: OFF. BURST/GATE/CONT: CONT. UPPER LEVEL: +4V. LOWER LEVEL: −4V. PERIOD VERNIER: Adjust for 10 μs square wave	Verify continuous output when TRIG/GATE INPUT is shorted.
2			BURST/CONT/GATE: GATE	Verify quiescent output when TRIG/GATE INPUT is shorted.
3	External Trigger Burst	Scope and External source of 1 kHz TTL connected to TRIG/ GATE INPUT	BURST/CONT/GATE: BURST. BURST Switches: 00000	Verify a single pulse at 1 kHz rate.
4			BURST Switches: 00001	Verify a single pulse at 1 kHz rate.
5			BURST Switches: 00002	Verify two pulses every 1 kHz.
6			BURST Switches: 00003 through 00009	Verify correct number of pulses for each BURST Switch position.
7			BURST Switches: 00005. BURST/CONT/GATE: CONT. PERIOD: 20 ns / 200 ns. PERIOD VERNIER: Adjust for 100 ns period.	100 ns period
8		Scope and External Source of 100 kHz TTL connected to TRIG/ GATE INPUT.	BURST/CONT/GATE: BURST. PERIOD VERNIER: See results.	Rotate period vernier until six pulses appear or runs continuously. Then, rotate vernier slightly cw until five pulses appear.
9		Counter	BURST/CONT/GATE: CONT	Verify <66 ns period square wave.
10	Burst Count 99999	Counter: Set to Totalization (External source disconnected)	BURST/CONT/GATE: BURST PERIOD: 200 ns / 2μs. PERIOD VERNIER: cw. BURST Switches: 99999. MAN TRIG: press in.	Counter displays 99999 each time MAN TRIG is pressed. (Refer to counter operator's manual for use.)

Table 6-3. Burst Board Verification (Continued)

Step	Check	Tester	Control Setting	Desired Results
11	Burst Count 66666		BURST Switches: 66666. MAN TRIG: press in.	Counter displays 66666 each time MAN TRIG is is pressed.
12	Burst Count 33333		BURST Switches: 33333. MAN TRIG: press in.	Counter displays 33333 each time MAN TRIG is pressed.
13	Burst Count 1		BURST Switches: 00000. MAN TRIG: press in.	Counter displays 1 each time MAN TRIG is pressed.
14	Double Pulse		DELAY: 100 ns / 1μs. DELAY VERNIER: cw. WIDTH: 1μs / 10μs. BURST Switches: 00005. DBL PULSE: ON. MAN TRIG: press in.	Counter displays 10 each time MAN TRIG is pressed.
15	External Trigger Check	Scope. Horizontal: 5μs/div. Vertical: 2V/div. External Source of 100 kHz TTL connected to TRIG/ GATE INPUT.	PERIOD: TRIG. WIDTH VERNIER: Rotate from cw to ccw.	Verify a pulse with variable width.
16			BURST/CONT/GATE: CONT.	Verify a pulse with variable width.
17			BURST/CONT/GATE: GATE	Verify a pulse with variable width.
18	Manual Trigger Check	Scope. Horiz: 100μs/div. Vert: 2V/div.	PERIOD: MAN TRIG. WIDTH: 10μs / 100μs. WIDTH VERNIER: Rotate ccw to cw. MAN TRIG: press in.	Verify a pulse with variable width each time MAN TRIG is pressed.
19			BURST/CONT/GATE: CONT.	Verify a pulse with variable width each time MAN TRIG is pressed.
20			BURST/CONT/GATE: BURST	Verify a pulse with variable width each time MAN TRIG is pressed.

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

Drawing	Drawing No.
Instrument Schematic	0004-00-0186
Chassis Assembly	0102-00-1016
Chassis Parts Lists	1101-00-1016
Generator Board Schematic	0103-00-0987
Generator Board Assembly	0101-00-0987
Generator Board Parts List	1100-00-0987
Burst Board Schematic	0103-00-0989
Burst Board Assembly	0101-00-0989
Burst Board Parts List	1100-00-0989

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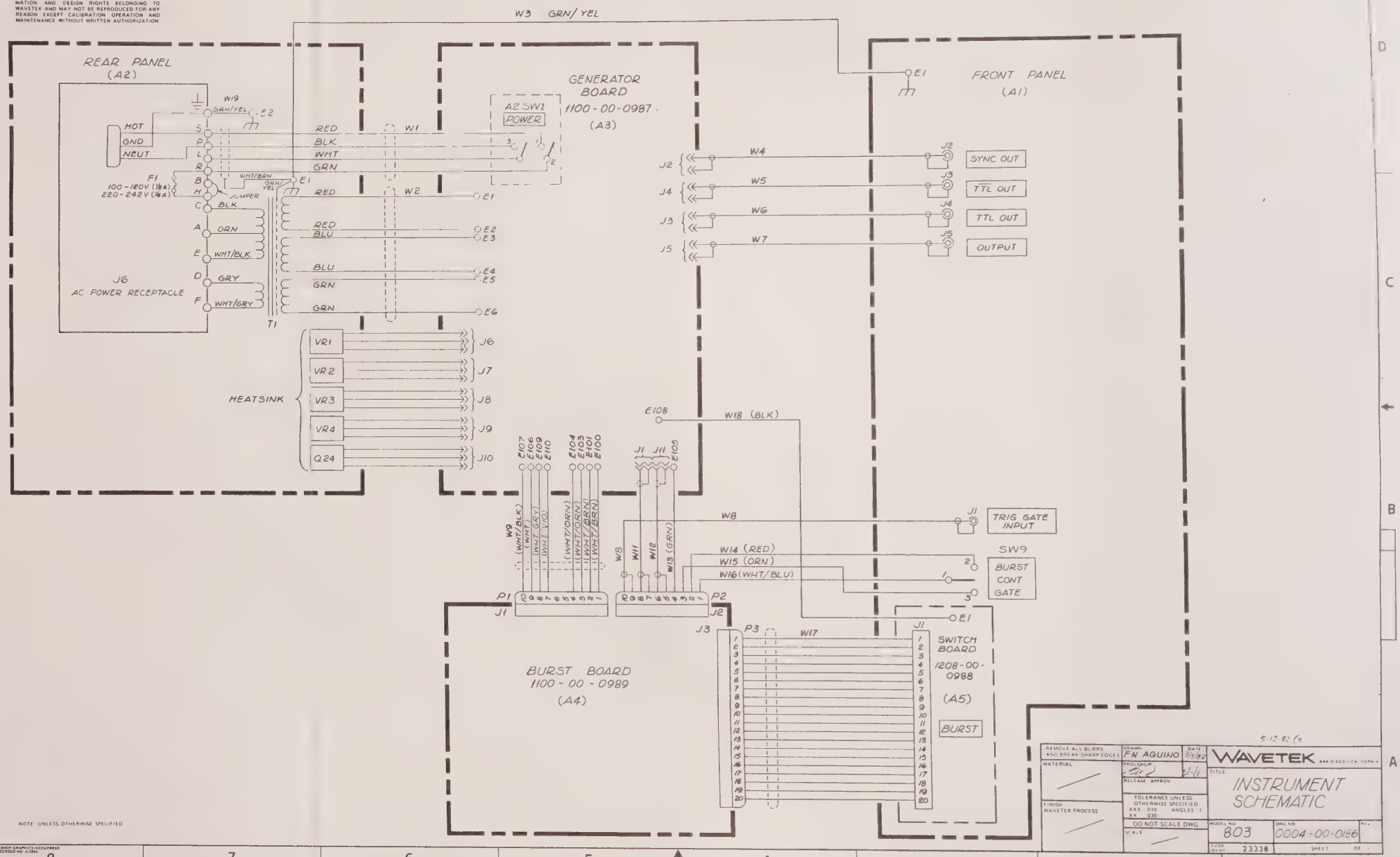

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN FN AQUINO	DATE 3/3/82	WAVETEK
MATERIAL	PROJ MGR		TITLE INSTRUMENT SCHEMATIC
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030		
	DO NOT SCALE DWG		MODEL NO 803
	SCALE		DWG NO 0004-00-0186
			CODE IDENT 23338
			SHEET OF

5-12-82 (9)

BISHOP GRAPHICS/ACCUPRESS REORDER NO A1994

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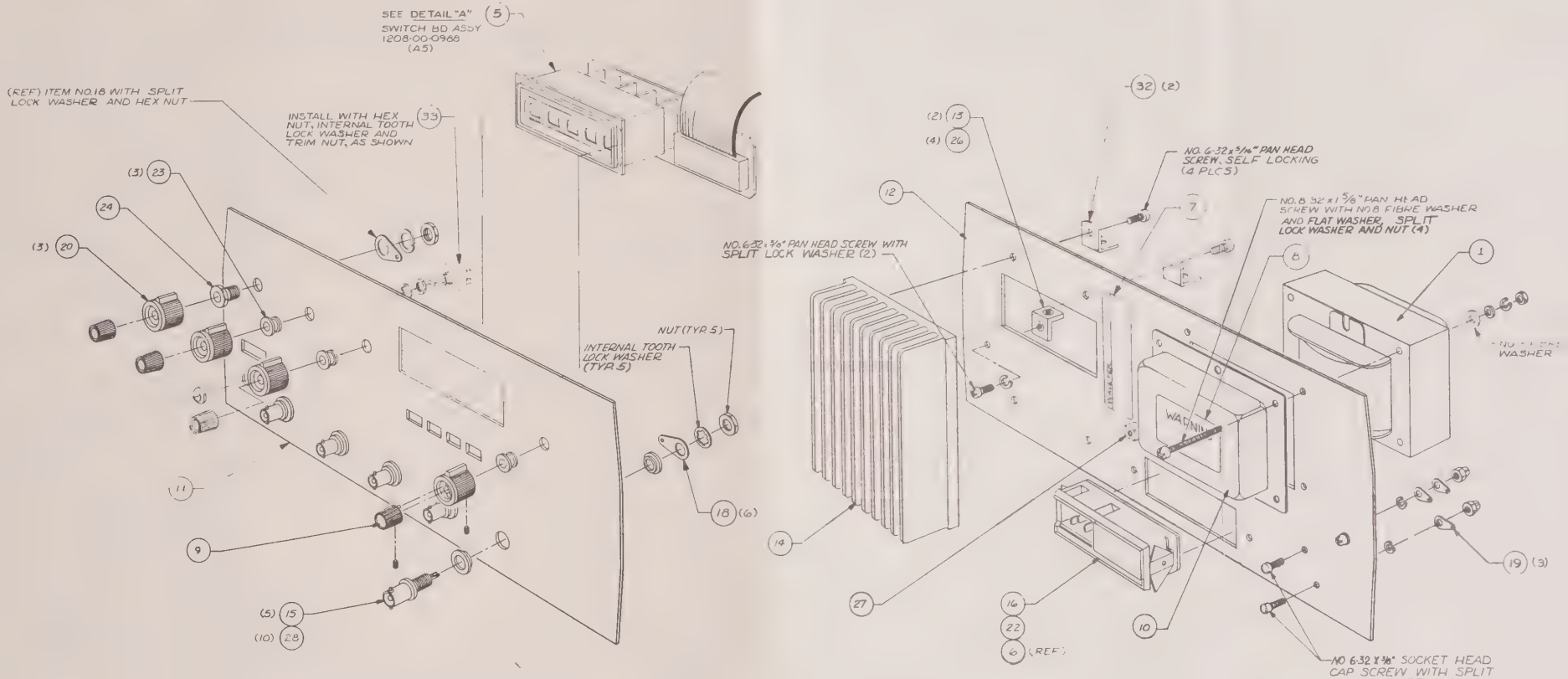
REV	ECN	BY	DATE	APP


SEE DETAIL "A" (5)
SWITCH BD ASSY
1208-00-0968
(A5)
(REF) ITEM NO.18 WITH SPLIT LOCK WASHER AND HEX NUT
INSTALL WITH HEX NUT, INTERNAL TOOTH LOCK WASHER AND TRIM NUT, AS SHOWN (33)
(3) (23)
24
(3) (20)
11
9
(5) (15)
(10) (28)
NUT (TYP.5)
INTERNAL TOOTH LOCK WASHER (TYP.5)
18 (6)
FRONT PANEL ASSY (A1)
(2) (13)
(4) (26)
32 (2)
NO. 6-32 x 5/16" PAN HEAD SCREW, SELF LOCKING (4 PLCS)
12
7
NO. 8-32 x 1 3/8" PAN HEAD SCREW WITH NO.8 FIBRE WASHER AND FLAT WASHER, SPLIT LOCK WASHER AND NUT (4)
8
1
NO. 6-32 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER (2)
14
27
16
22
6 (REF)
10
19 (3)
NO 6-32 X 3/8" SOCKET HEAD CAP SCREW WITH SPLIT LOCK WASHER AND NO.6 LOCK NUT (2 PLCS)
REAR PANEL ASSY (A2)
(REF) SWITCH BD ASSY
(REF) BACK SIDE FRONT PANEL
APPLY DOW CORNING SILICONE RUBBER SEALANT # 732-7 (BLK) TO BACK SIDE OF PANEL AND AROUND SWITCH, AS INDICATED
DETAIL A
SWITCH BD ASSY TO FRONT PANEL INSTALLATION

3. FOR SUB-ASSEMBLY REFERENCE DESIGNATORS AND WIRING HOOK-UP REF. INSTRUMENT SCHEMATIC DWG. NO. 0004-00-0186.

2. CABLES OBTAINED FROM CHASSIS CABLE KIT P/N 1207-00-1021

1. SEE PARTS LIST NO. 1101-00-1016

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 7-1-80	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 803
	SCALE		DWG NO 0102-00-1016 REV
			CODE IDENT 23338 SHEET 1 OF 2

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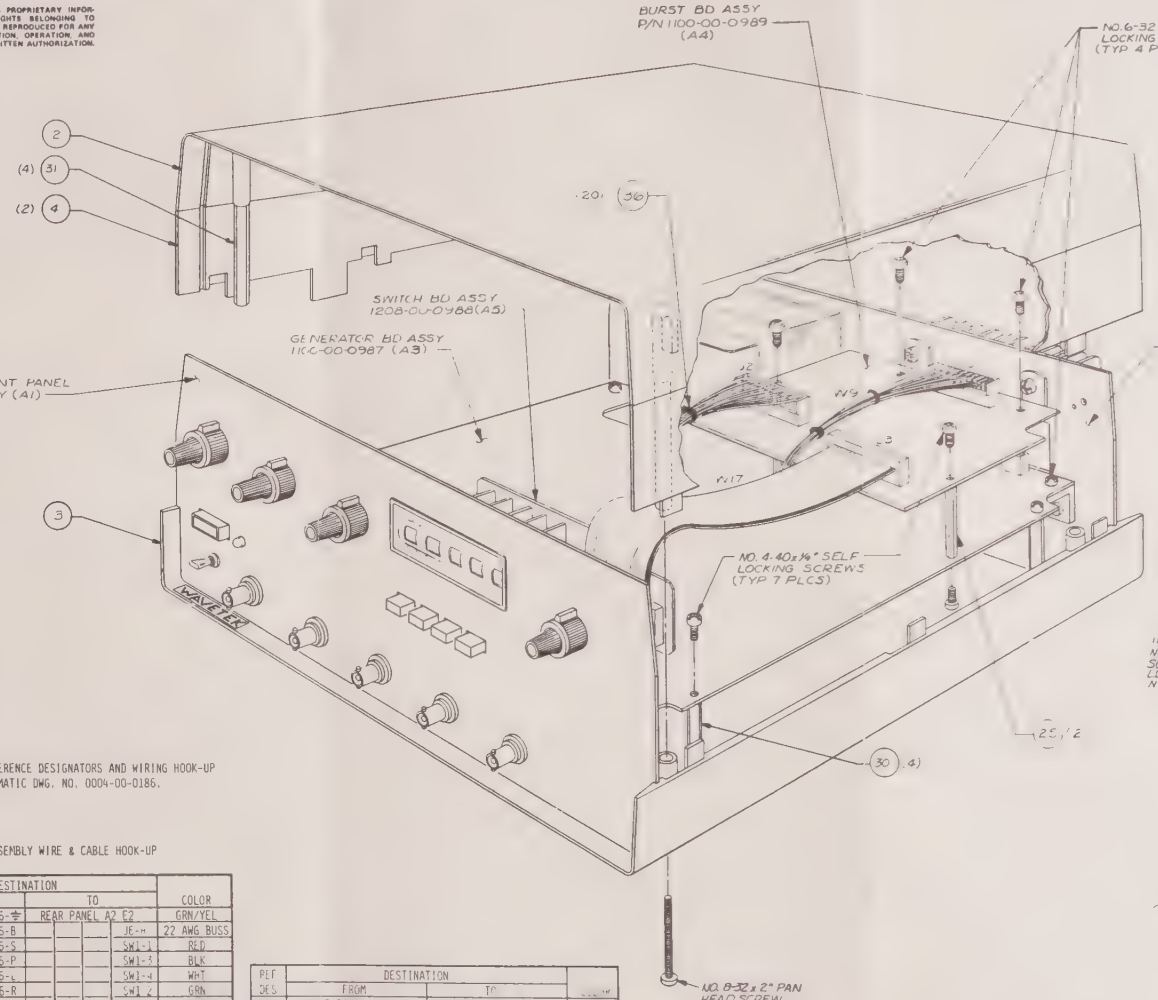
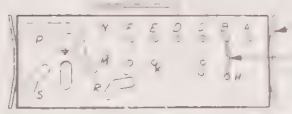
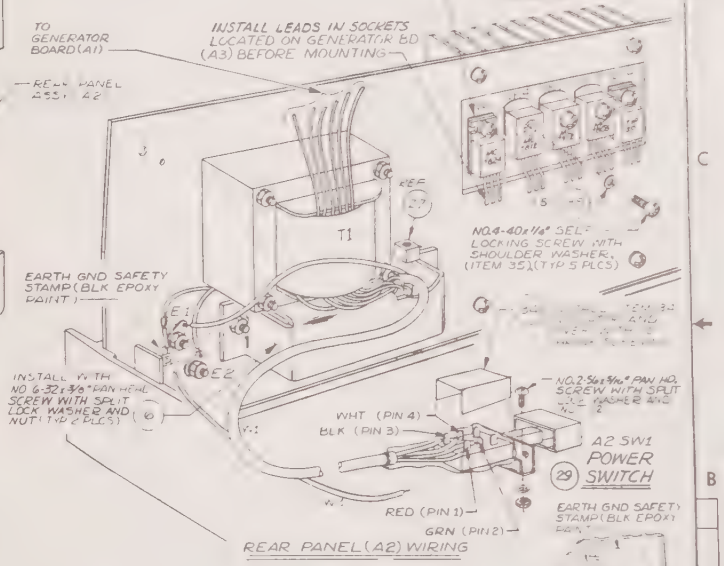
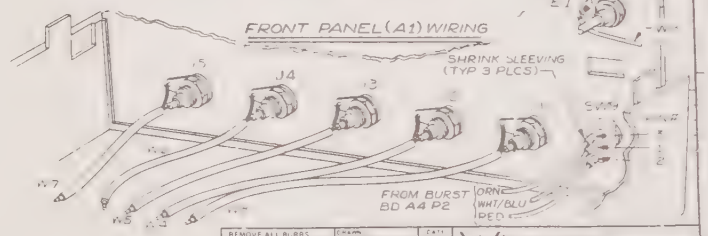





TO GENERATOR BOARD(A1)
REAR PANEL ASSY A2
INSTALL LEADS IN SOCKETS LOCATED ON GENERATOR BD (A3) BEFORE MOUNTING
NO.4-40 x 1/4" SELF LOCKING SCREW WITH SHOULDER WASHER, (ITEM 35)(TYP 5 PLCS)
EARTH GND SAFETY STAMP(BLK EPOXY PAINT)
INSTALL WITH NO.6-32 x 3/8" PAN HEAD SCREW WITH SPLIT LOCK WASHER AND NUT (TYP 2 PLCS)
NO.2-56 x 3/16" PAN HD. SCREW WITH SPLIT LOCK WASHER AND
WHT (PIN 4)
BLK (PIN 3)
A2 SW1 POWER SWITCH
RED (PIN 1)
GRN (PIN 2)
REAR PANEL(A2) WIRING



FOR SUB-ASSEMBLY REFERENCE DESIGNATORS AND WIRING HOOK-UP REF. INSTRUMENT SCHEMATIC DWG. NO. 0004-00-0186.

CHASSIS ASSEMBLY WIRE & CABLE HOOK-UP

REF DES	DESTINATION FROM	DESTINATION TO	COLOR
W19	REAR PANEL A2 J6-⏚	REAR PANEL A2 E2	GRN/YEL
NONE	J6-B	J6-M	22 AWG BUSS
W1	J6-S	SW1-1	RED
	J6-P	SW1-3	BLK
	J6-L	SW1-4	WHT
	REAR PANEL A2 J6-R	SW1-2	GRN
	W1 SHIELD	E1	WHT/BRN
NONE	REAR PANEL A2 T1	J6-C	BLK
		J6-A	ORN
		J6-E	WHT BLP
		J6-D	GRY
		J6-F	WHT/GRY
	REAR PANEL A2 E1		GRN/YEL
W2	GEN BD A3 E1		RED
	A3 E2		RED
	A3 E3		BLU
	A3 E4		BLU
	A3 E5		GRN
	A3 E6		GRN
W3	REAR PANEL A2 E1	FRONT PANEL A1 E1	GRN/YEL

REF DES	DESTINATION FROM	DESTINATION TO	COLOR
W4	FRONT PANEL A1 J2	GEN BD A3 J1	GRY
W5			
W6			
W7	FRONT PANEL A1 J5		GRY
W15	SWITCH BD A5 E1	GEN BD A3 E105	BLK
W9	GEN BD A3	BURST BD A4 J1	N/A
W10	FRONT PANEL A1 SW9-1		WHT B...
W14	A1 SW9-2		RED
W15	A1 SW9-3	J2-3	ORN
W8	FRONT PANEL A1 J1	J2	GRY
W13	GEN BD A3 E105	J2	GRN
W12	A3 J11	J2	GRY
W11	GEN BD A3 J1	BURST BD A4 J2	GRY
W17	SWITCH BD A5 J1	BURST BD A4 J3	N/A

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030
DO NOT SCALE DWG
SCALE NONE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: ASSEMBLY CHASSIS

MODEL NO 803
DWG NO 0102-00-1016
REV
CODE IDENT 23338
SHEET 2 OF 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, CHASSIS	0102-00-1016	WVTK	0102-00-1016	1
1	TRANSFORMER	803-0055	WVTK	1204-00-0055	1
2	ASSY, TOP COVER	1206-00-1013	WVTK	1206-00-1013	1
3	ASSY, BOTTOM COVER	1206-00-1014	WVTK	1206-00-1014	1
NONE	CHASSIS CABLE KIT	803-1021	WVTK	1207-00-1021	1
5	PCA, SWITCH BOARD	803-0988	WVTK	1208-00-0988	1
17	INSULATOR, MICA	142-311	WVTK	1400-00-2080	5
4	EXPANDER	180-301	WVTK	1400-00-5010	2
6	SHIELD, PWR	1400-00-6210	WVTK	1400-00-6210	1
8	LABEL, WARNING	1400-00-6940	WVTK	1400-00-6940	1
10	END BELL	1400-00-6984	WVTK	1400-00-6984	1
12	PANEL, REAR	1400-00-7853	WVTK	1400-00-7853	1
13	BRKT, SUPT	1400-00-7883	WVTK	1400-00-7883	2
14	HEAT SINK REF: 3200-06-0002	1400-00-7899	WVTK	1400-00-7899	1
34	INSULATOR, PWR SWITCH REF: 1600-99-0001	1400-00-8370	WVTK	1400-00-8370	2
7	I.D. LABEL	1400-00-9090	WVTK	1400-00-9090	1
9	COAX KNOB SET	1400-01-1429	WVTK	1400-01-1429	1

WAVETEK PARTS LIST	TITLE ASSY, CHASSIS	ASSEMBLY NO. 1101-00-1016 PAGE: 1	REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	QTY: 1: 2400-01-0009				
11	FRONT PANEL	1400-01-4910	WVTK	1400-01-4910	1
15	BNC CONN	KC-7946	KING	2100-01-0002	5
16	RECEPTACLE	6VJ1	CORCM	2100-03-0026	1
18	SOLDER LUG	1497	SMITH	2100-04-0012	6
19	SOLDER LUG	1485-6	SMITH	2100-04-0025	3
20	COAX KNOB SET	RB-67-1-SB+0-M-9	ROGAN	2400-01-0009	3
22	FUSE, 1/2A, 250V	313.500	LITFU	2400-05-0010	1
36	TY-WRAP	TY-523M	TB	2800-00-0006	20
23	BUSHING NYLINER	4L2FF	THOMN	2800-01-0002	3
24	BEARING, PANEL	119	SMITH	2800-01-0004	1
31	STANDOFF, MALE/FEMALE 1.750 H, .250 HEX 8-32	1475-M03-F05-832	UNICP	2800-02-0010	4
25	STANDOFF 1.750 H, .250 HEX 4-40	P-609-M03-F05-440	WVTK	2800-02-0016	2
30	STANDOFF, MALE/FEMALE 1.875H, .250 HEX, 4-40	1479-M03-F05-440	UNICP	2800-02-0023	4
26	INSERT # 6	74-11-106-13	SOTCO	2800-09-0017	4

WAVETEK PARTS LIST	TITLE ASSY, CHASSIS	ASSEMBLY NO. 1101-00-1016	REV
		PAGE: 2	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
27	FAST, CHASSIS	1591-C11	USECO	2800-09-0022	1
35	WASHER	B51547F015	MOT	2800-11-0015	5
28	WASHER, SHOULDER	2668	SMITH	2800-27-0004	10
32	ANGLE BRACKET	3000-00-0091	WVTK	3000-00-0091	2
29	SWITCH ASSY PB	5102-00-0008	WVTK	5102-00-0008	1
33	SWITCH, TOGGLE	7103P3NHZQE	C&K	5106-00-0031	1

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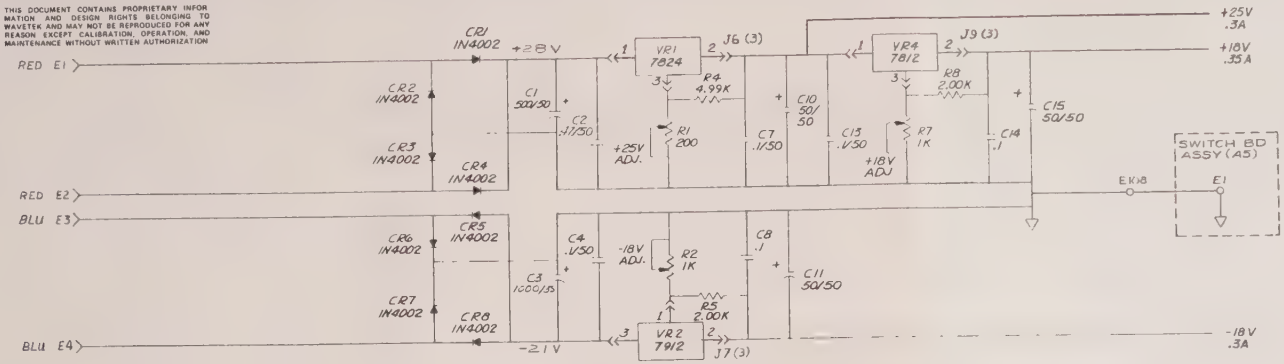
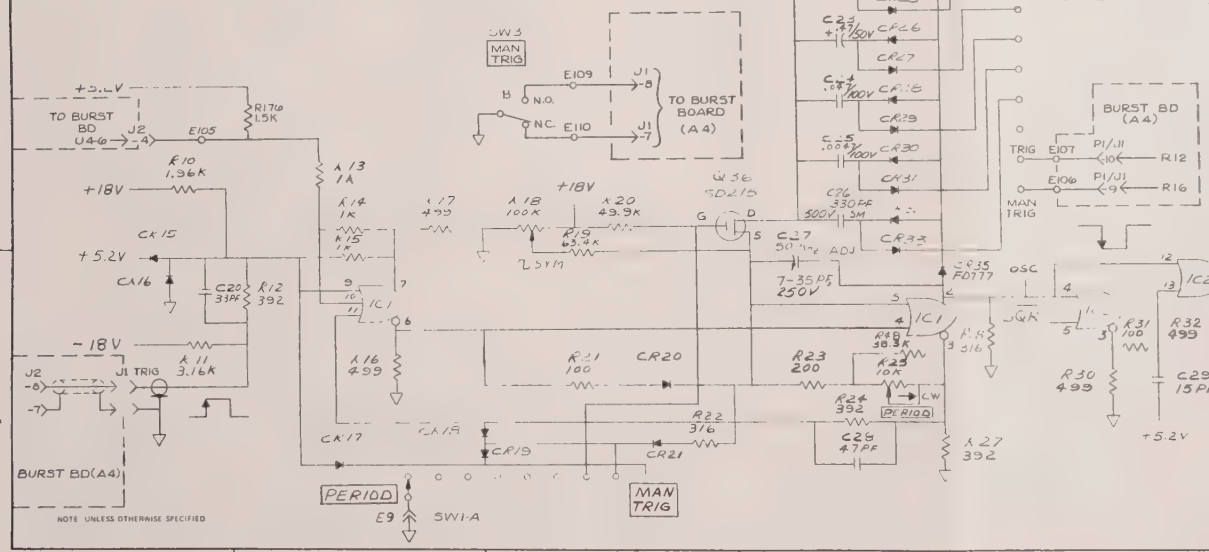
LAST REF. DES. USED
R 176
CR 74
IC 7
Q 36
VR 4
SW 7
C 74
L 10
J 11
E 110
N2W & P8W NOT USED
E102 NOT USED





REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN J.COOPER	DATE 3/29/82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL			TITLE SCHEMATIC GENERATOR BOARD (A3)
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		
	DO NOT SCALE DWG		MODEL NO. 803 DWG NO. 000 00-0987 REV.
			IN 23338 SHEET 1 OF 2

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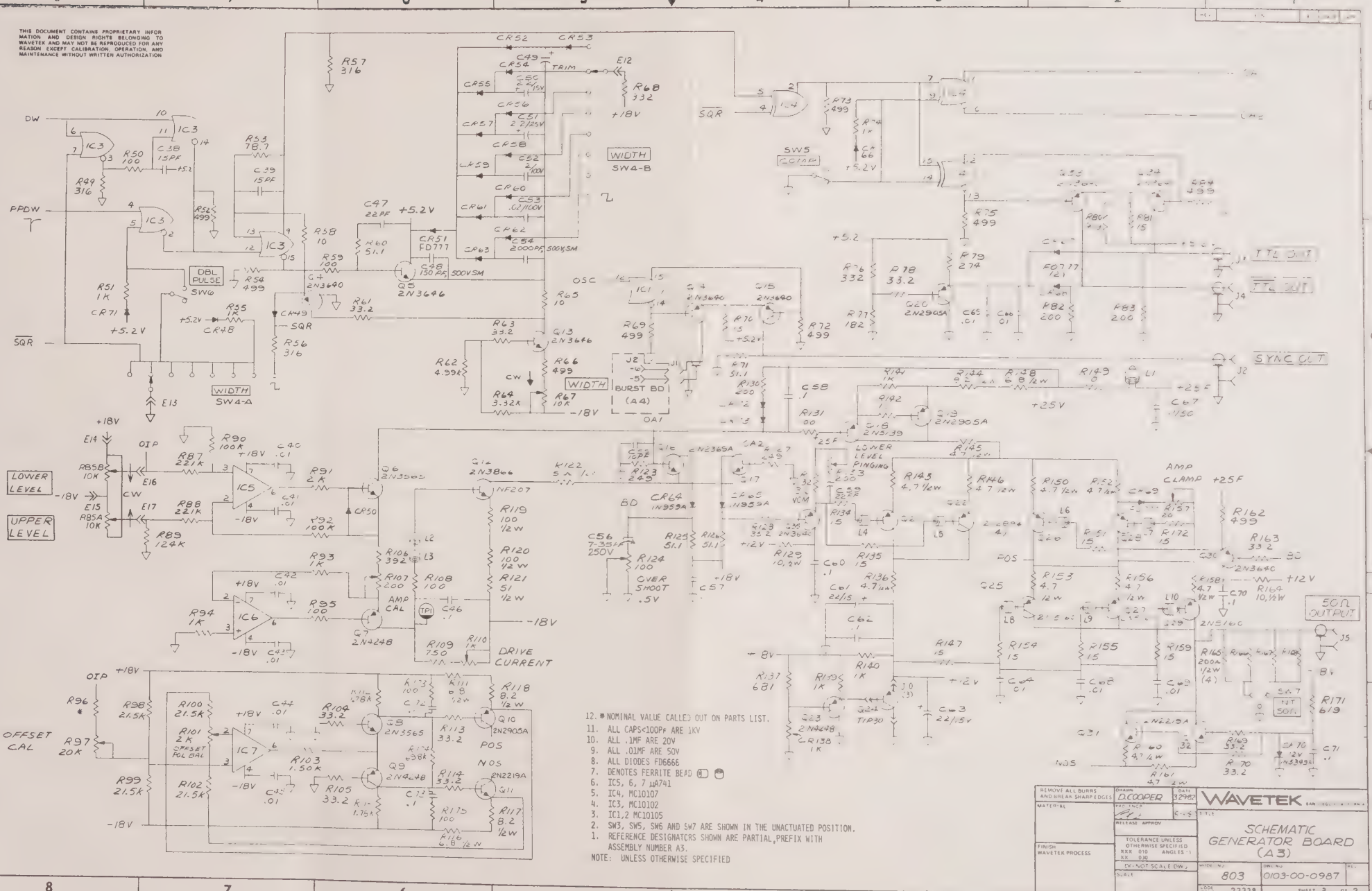

12. * NOMINAL VALUE CALLED OUT ON PARTS LIST.
11. ALL CAPS<100PF ARE 1KV
10. ALL .1MF ARE 20V
9. ALL .01MF ARE 50V
8. ALL DIODES FD6666
7. DENOTES FERRITE BEAD
6. IC5, 6, 7 μA741
5. IC4, MC10107
4. IC3, MC10102
3. IC1,2 MC10105
2. SW3, SW5, SW6 AND SW7 ARE SHOWN IN THE UNACTUATED POSITION.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY NUMBER A3.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D.COOPER
DATE 3/29/82
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES ±1° XX .030
DO NOT SCALE DWG.
SCALE

WAVETEK

SCHEMATIC GENERATOR BOARD (A3)

MODEL NO 803
DRAWING NO 0103-00-0987 REV
CAGE IDENT 23338
SHEET 2 OF 2

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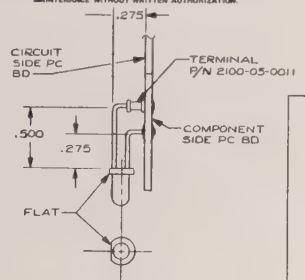
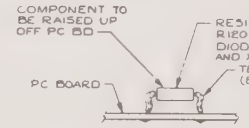


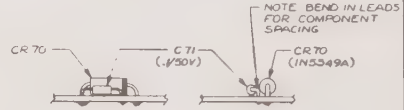
DETAIL "A"
LED INSTALLATION

SPRING SOCKET P/N 2100-03-0037 WITH COAX SOCKET P/N 2100 03 0038 (TYP 6 PLCS, REF J1 THRU J3 AND J11)

MOLEX SOCKETS P/N 2100-03-0047 (5 PLCS)


COMPONENT TO BE RAISED UP OFF PC BD
RESISTOR (REF R119, R120, R144, R148) AND DIODE (REF CR64, CR65) AND XSISTOR (REF Q12)
TEFLON SLEEVING (BOTH LEADS)
PC BOARD

DETAIL "B" (REF) [6]
COMPONENT LEAD INSULATION



DETAIL "C"
INSTALLATION-"CR70","C71"

SEE DETAIL "C"

(REF) POWER SWITCH MTG LOCATION FARSIDE PC BD

LED INSTALLATION FARSIDE SEE DETAIL "A"

MALE AMP PIN P/N 2100-05-0020

BUTTON (BLACK) P/N 5103-04-0003 (4 PLCS)

SWITCH ASSY P/N 5103-00-0025 WITH TEFLON SPACERS FOR PROPER WEIGHT FROM PC BOARD (SPACER DIMENSIONS .090 x .190)

(REF) MTG BRKT LOCATION NEAR SIDE SEE SHEET 2

[6] HEATSINK FINS ON Q32 MUST BE SEPARATED TO AVOID CONTACT WITH "R85" POT ON BRACKET.

[5] THESE 7 COMPONENTS (R119, R120, R144, R148, CR64, CR65 & Q12) ARE TO BE RAISED UP OFF PC BOARD AND LEADS ARE TO BE SLEEVED WITH NO. 20 TEFLON SLEEVING (REF. DETAIL "B").
NOTE: Q12 - SLEEVE ONLY EMITTER & COLLECTOR LEADS.

[4] INSTALL TALL TRANSIPAD (P/N 2800-11-0004) ON BASE OF THESE COMPONENTS (8 PLCS) - Q10, Q11, Q19, Q32, (Q25, Q27 & Q29 - REMOVE ONE LEG FROM EACH TRANSIPAD TO CLEAR FERRITE BEAD ON BASE LEAD ON THESE 3 COMPONENTS), (Q31 - TRIM SIDE OF TRANSIPAD ON THIS COMPONENT TO CLEAR 1/2 W. RESISTOR),

[3] INSTALL SHORT TRANSIPAD (P/N 2800-11-0003) ON BASE OF THIS COMPONENT - Q20 (1 PLC).

[2] INSTALL 2 FERRITE BEADS (P/N 3100-00-0001) ON BASE LEAD OF THIS COMPONENT - Q12 (1 PLC)
NOTE: NO TRANSIPAD ON THIS COMPONENT.

[1] INSTALL 1 FERRITE BEAD (P/N 3100-00-0001) ON BASE LEAD OF THESE COMPONENTS - Q21, Q22, Q25, Q26, Q27, Q28, Q29 (7 PLCS).

4. * NOMINAL VALUE CALLED OUT ON PARTS LIST.

3. FOR SUB-ASSEMBLY REFERENCE DESIGNATORS AND WIRING HOOK-UP REF. INSTRUMENT SCHEMATIC DWG. NO. 0004-00-0186.

2. CABLES ARE OBTAINED FROM CHASSIS CABLE KIT P/N 1207-00-1021

1. SEE PARTS LIST 1100-00-0987

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 1-12-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR	5/3/82	TITLE ASSEMBLY, GENERATOR BOARD (A3)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO 803	DWG NO 0101-00-0987 REV
	SCALE 2/1	CODE IDENT 23338	SHEET 1 OF 2

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REV	ECN	BY	DATE	APP

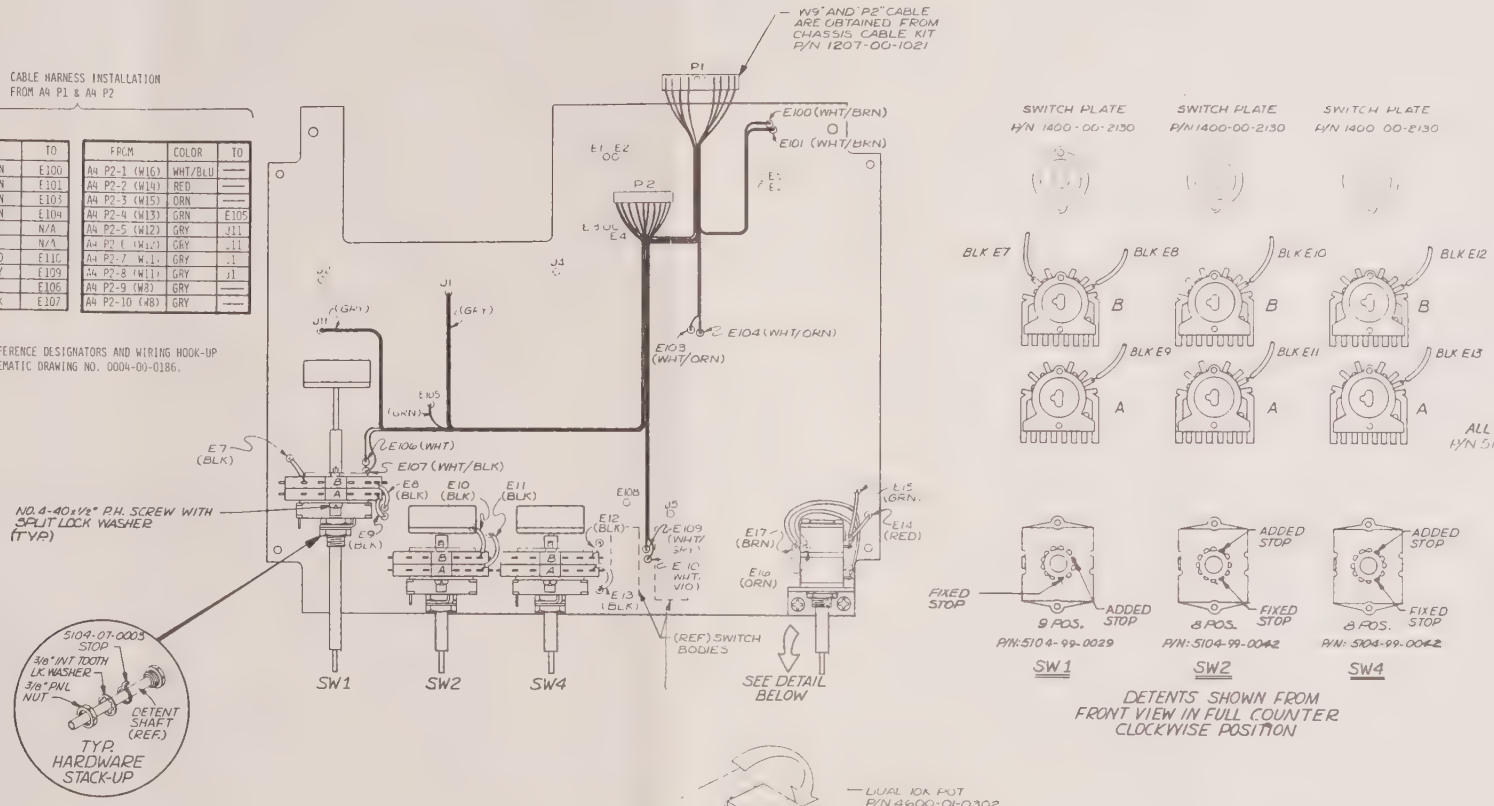
CABLE HARNESS INSTALLATION
FROM A4 P1 & A4 P2

W9

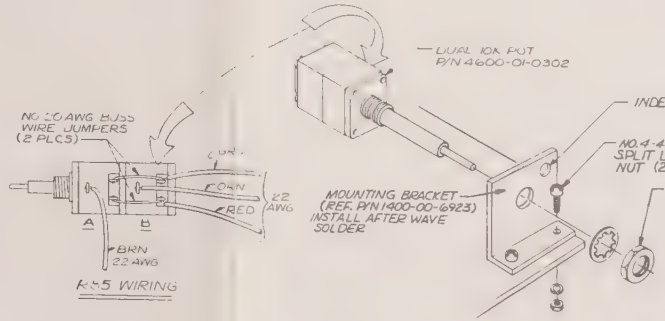
FROM	COLOR	TO
A4 P1-1	WHT/BRN	E100
A4 P1-2	WHT/BRN	E101
A4 P1-3	WHT/ORN	E103
A4 P1-4	WHT/ORN	E104
A4 P1 5	N/A	N/A
A4 P1-6	N/A	N/A
A4 P1-7	WHT/VIO	E110
A4 P1 8	WHT/GRY	E109
A4 P1-9	WHT	E106
A4 P1-10	WHT/BLK	E107

FROM	COLOR	TO
A4 P2-1 (W16)	WHT/BLU	—
A4 P2-2 (W14)	RED	—
A4 P2-3 (W15)	ORN	—
A4 P2-4 (W13)	GRN	E105
A4 P2-5 (W12)	GRY	J11
A4 P2 6 (W11)	GRY	J11
A4 P2-7 W10	GRY	J1
A4 P2-8 (W11)	GRY	J1
A4 P2-9 (W8)	GRY	—
A4 P2-10 (W8)	GRY	—

FOR SUB-ASSEMBLY REFERENCE DESIGNATORS AND WIRING HOOK-UP REF. INSTRUMENT SCHEMATIC DRAWING NO. 0004-00-0186.



DETENTS SHOWN FROM FRONT VIEW IN FULL COUNTER CLOCKWISE POSITION


DUAL 10K POT P/N 4600-01-0302
INDEX HOLE
NO.4-40 x 5/16" P.H. SCREW WITH SPLIT LOCK WASHER AND NUT (2)
NO. 20 AWG BUSS WIRE JUMPERS (2 PLCS)
MOUNTING BRACKET (REF. P/N 1400-00-6923) INSTALL AFTER WAVE SOLDER
3/8" PNL NUT AND INT. TOOTH LOCK WASHER
ORN
RED
22 AWG
BRN
22 AWG
K45 WIRING

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 9-27-77	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ MGR		TITLE: ASSEMBLY GENERATOR BOARD (A3)
	RELEASE APPRV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XX ± .010 ANGLES ± 1° .XXX ± .005		MODEL NO 803
	DO NOT SCALE DWG		DWG NO 0101-00-0987 REV
	SCALE		CODE IDENT 23338 SHEET 2 OF 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, GENERATOR	0101-00-0987	WVTK	0101-00-0987	1
NONE	SCHEMATIC, GENERATOR	0103-00-0987	WVTK	0103-00-0987	1
NONE	PLATE, SW	008-004	WVTK	1400-00-2130	3
NONE	BRACKET	1400-00-6923	WVTK	1400-00-6923	1
C55	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	1
C40 C41 C42 C43 C44 C45 C64 C65 C66 C68 C69	CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	11
C13 C14 C16 C17 C18 C19 C4 C46 C57 C58 C6 C60 C62 C67 C7 C70 C71 C72 C73 C8 C9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	21
C29 C30 C38 C39	CAP, CER, 15PF, 1KV	DD-150	CRL	1500-01-5011	4
C31 C47 C59	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	3
C20	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	1
C28	CAP, CER, 47PF, 1KV	DD-470	CRL	1500-04-7011	1
C37 C48	CAP, MICA, 150PF, 500V	DM15-151J	ARCO	1500-11-5100	2
C36 C54	CAP, MICA, 2000PF, 500V	DM19-202J	ARCO	1500-12-0200	2
C26	CAP, MICA, 330PF, 500V	DM15-331J	ARCO	1500-13-3100	1
C3	CAP, ELECT, 1000MF/35V	CRE-SERIES-1000/35	CAPAR	1500-31-0202	1

WAVETEK PARTS LIST	TITLE PCB GENERATOR	ASSEMBLY NO. 1100-00-0987 PAGE. 1	REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	RADIAL LEAD, SP .30				
C5	CAP,ELECT,1900MF,15V	39D198G015GL4	SPRAG	1500-31-9201	1
C10 C11 C15	CAP,ELECT,50MF,50V	500D506G050DD7	SPRAG	1500-35-0003	3
C1	CAP,ELECT,500MF,50V	39D507G050GL4	SPRAG	1500-35-0103	1
C35 C53	CAP,MYLR,.02MF,100V	BA1B203F	IMB	1500-42-0304	2
C34 C52	CAP,MYLR,.2MF,100V	BA1B204F	IMB	1500-42-0404	2
C25	CAP,MYLR,.0047MF100V	WMF-1D47	CDE	1500-44-7214	1
C24	CAP,MYLR,.047MF,100V	WMF-1S47	CDE	1500-44-7304	1
C27 C56	VARI,7-35PF,250V	7S-TRIKO-02 7/35 PF	TRIKO	1500-53-5000	2
C33 C51	CAP,TANT,2.2MF,25V	196D225X9025HA1	SPRAG	1500-72-2502	2
C12 C32 C50 C61 C63	CAP,TANT,22MF,15V	196D226X9015KA1	SPRAG	1500-72-2601	5
C2 C23	CAP,TANT,.47MF,50V	150D474X9050B2	SPRAG	1500-74-7403	2
C22	CAP,TANT,4.7MF,35V	150D475X9035B2	SPRAG	1500-74-7502	1
C21	CAP,TANT,47MF,20V	196D476X9020PE4	SPRAG	1500-74-7601	1
NONE	GENERATOR BOARD	1700-00-0987	WVTK	1700-00-0987	1
NONE	SPRING SOCKET	3-330-808-9	AMP	2100-03-0037	6
J1 J11 J2 J3 J4 J5	COAX SOCKET	226287-2	AMP	2100-03-0038	6
J10 J6 J7 J8 J9	SOCKET	10-18-2031	MOLEX	2100-03-0047	5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
E108	PIN, MALE	61182-2	AMP	2100-05-0020	1
NONE	HEAT SINK	207	WAKE	2800-11-0001	4
NONE	TRANSIPAD	10123N	METRS	2800-11-0003	1
NONE	TRANSIPAD	10160	METRS	2800-11-0004	8
NONE	HEATSINK	209	WAKE	2800-11-0008	5
NONE	HEATSINK	203 CB	WAKE	2800-11-0009	4
L10 L2 L3 L4 L5 L6 L7 L8 L9	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	9
L1	BALUN CORE	2873000902	FARIT	3100-00-0002	1
R124 R3	POT, TRIM, 100	91AR100	BECK	4600-01-0103	2
R110 R2 R7	POT, TRIM, 1K	91AR1K	BECK	4600-01-0209	3
R18	POT, TRIM, 100K	91AR100K	BECK	4600-01-0402	1
R157	POT, TRIM, 20	91AR20	BECK	4600-02-0000	1
R1 R107 R133	POT, TRIM, 200	91AR200	BECK	4600-02-0101	3
R101	POT, TRIM, 2K	91AR2K	BECK	4600-02-0201	1
R97	POT, TRIM, 20K	91AR20K	BECK	4600-02-0301	1
R85	POT, DUAL, 10K, LINER	4600-21-0302	WVTK	4600-21-0302	1
R25	POT, CONT, 10K	4609-71-0309	WVTK	4609-71-0309	1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	FROM: 4600-01-0312				
R46 R67	POT, CONT, 10K FROM: 4600-01-0312	4609-71-0310	WVTK	4609-71-0310	2
R129 R164	RES, C, 1/2W, 5%, 10	RC20GF-100	STKPL	4700-25-0100	2
R136 R143 R145 R146 R150 R152 R153 R156 R158 R160 R161	RES, C, 1/2W, 5%, 4.7	RC20GF-4R7	STKPL	4700-25-0479	11
R121 R122	RES, C, 1/2W, 5%, 51	RC20GF510J	STKPL	4700-25-0510	2
R111 R116 R148	RES, C, 1/2W, 5%, 6.8	RC20GF-6R8	STKPL	4700-25-0689	3
R117 R118 R144	RES, C, 1/2W, 5%, 8.2	RC20GF-8R2	STKPL	4700-25-0829	3
R119 R120	RES, C, 1/2W, 5%, 100	RC20GF101J	STKPL	4700-25-1000	2
R108 R131 R173 R175 R21 R31 R39 R50 R59 R95	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	10
R13 R138 R139 R14 R140 R141 R15 R51 R55 R74 R93 R94	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	12
R90 R92 R96T	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	3
R142 R149 R35 R44 R58 R65	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	6
R29	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	1
R89	RES, MF, 1/8W, 1%, 124K	RN55D-1243F	TRW	4701-03-1243	1

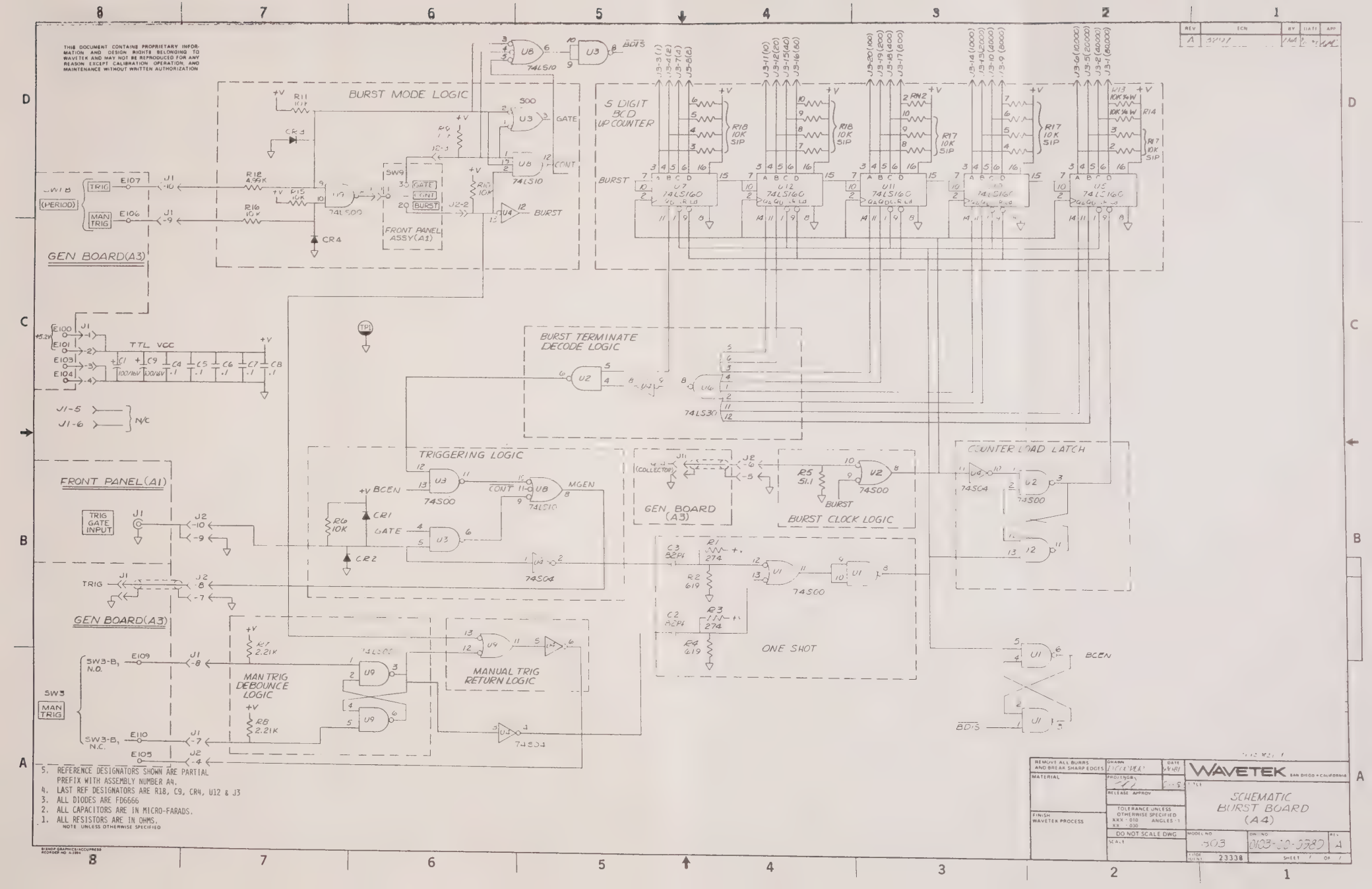
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R103 R176	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	2
R134 R135 R147 R151 R154 R155 R159 R172 R70 R81	RES, MF, 1/8W, 1%, 15	RN55D-15R0F	TRW	4701-03-1509	10
R112 R115	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	2
R77	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1
R10	RES, MF. 1/8W, 1%, 1.96K	RN55D-1961F	TRW	4701-03-1961	1
R130 R23 R82 R83	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	4
R5 R8 R91	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	3
R100 R102 R98 R99	RES, MF, 1/8W, 1%, 21.5K	RN55D-2152F	TRW	4701-03-2152	4
R87 R88	RES, MF, 1/8W, 1%, 221K	RN55D-2213F	TRW	4701-03-2213	2
R123 R127	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	2
R79	RES, MF, 1/8W, 1%, 274	RN55D-2740F	TRW	4701-03-2740	1
R132 R22 R28 R33 R36 R37 R49 R56 R57	RES, MF, 1/8W, 1%, 316	RN55D-3160F	TRW	4701-03-3160	9
R11	RES, MF, 1/8W, 1%, 3.16K	RN55D-3161F	TRW	4701-03-3161	1
R47 R68 R76	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	3
R43 R64	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	2
R104 R105 R113 R114	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	13

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R128 R163 R169 R170 R40 R42 R61 R63 R78					
R48	RES, MF, 1/8W, 1%, 38.3K	RN55D-3832F	TRW	4701-03-3832	1
R106 R12 R24 R27 R9	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	5
R16 R162 R17 R30 R32 R45 R52 R54 R66 R69 R72 R73 R75 R84	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	14
R4 R41 R6 R62	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	4
R20	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R125 R126 R38 R60 R71	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	5
R171	RES, MF, 1/8W, 1%, 619	RN55D-6190F	TRW	4701-03-6190	1
R19	RES, MF, 1/8W, 1%, 63.4K	RN55D-6342F	TRW	4701-03-6342	1
R137	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	1
R174	RES, MF, 1/8W, 1%, 69.8K	RN55D-6982F	TRW	4701-03-6982	1
R109	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	1
R34 R53	RES, MF, 1/8W, 1%, 78.7	RN55D-78R7F	TRW	4701-03-7879	2
R80	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	1
R165 R166 R167 R168	RES, MF, 1/2W, 1%, 200	RN65D2000F	TRW	4701-23-2000	4
CR64 CR65	DIODE	1N959	SIEM	4801-01-0959	2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR70	DIODE	1N5349A	MOT	4801-01-5349	1
CR1 CR10 CR11 CR12 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9	DIODE	1N4002	FAIR	4801-02-0001	12
CR35 CR43 CR51 CR67 CR68 CR69	DIODE	FD777	FAIR	4807-02-0777	6
CR15 CR16 CR17 CR18 CR19 CR20 CR21 CR22 CR23 CR24 CR25 CR26 CR27 CR28 CR29 CR30 CR31 CR32 CR33 CR34 CR36 CR37 CR38 CR39 CR40 CR41 CR42 CR44 CR45 CR46 CR47 CR48 CR49 CR50 CR52 CR53 CR54 CR55 CR56 CR57 CR58 CR59 CR60 CR61 CR62 CR63 CR66 CR71 CR72 CR73 CR74	DIODE	1N4148	FAIR	4807-02-6666	51
CR13	LED	TIL-220	TI	4899-00-0006	1
Q11 Q31 Q32	TRANS	2N2219A	NSC	4901-02-2191	3
Q16 Q17	TRANS	2N2369A	MOT	4901-02-3691	2
Q21 Q22 Q26 Q28	TRANS	2N2894A	FAIR	4901-02-8941	4
Q10 Q19 Q20	TRANS	2N2905A	NSC	4901-02-9051	3
Q6 Q8	TRANS	2N3565	FAIR	4901-03-5650	2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q14 Q15 Q2 Q30 Q33 Q34 Q35 Q4	TRANS	2N3640	FAIR	4901-03-6400	8
Q1 Q13 Q3 Q5	TRANS	2N3646	NSC	4901-03-6460	4
Q12	TRANS	2N3866	MOT	4901-03-8660	1
Q23 Q7 Q9	TRANS	2N4248	FAIR	4901-04-2480	3
Q18	TRANS	2N5139	FAIR	4901-05-1390	1
Q25 Q27 Q29	TRANS	2N5160-18	MOT	4901-05-1600	3
Q24	TRANS	TIP-30	TI	4902-00-0300	1
Q36	TRANS	SD215DE	SIG	4902-00-2140	1
NONE	SWITCH ASSY	5103-00-0025	WVTK	5103-00-0025	1
NONE	BUTTON	J-52305-BLACK	CRL	5103-04-0003	4
NONE	WAFER	147-400	WVTK	5104-02-0015	6
NONE	SWITCH STOP	215-33-001-01-22	CTS	5104-07-0003	3
SW1	DETENT MOD FROM: 5104-01-0010	5104-99-0029	WVTK	5104-99-0029	1
SW2 SW4	DETENT, MOD FROM: 5104-01-0003	5104-99-0042	WVTK	5104-99-0042	2
IC5 IC6 IC7	IC	LM741CN	NSC	7000-07-4100	3
VR4	IC	MC7812CT	MOT	7000-78-1200	1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
VR1	IC	7824	FAIR	7000-78-2400	1
VR2	IC	7912	MOT	7000-79-1200	1
VR3	VOLTAGE REGULATOR	MA7805UC	FAIR	8000-78-0500	1
IC3	IC	MC10102	MOT	8001-01-0200	1
IC1 IC2	IC	MC10105	MOT	8001-01-0500	2
IC4	IC	MC10107	MOT	8001-01-0700	1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REV ECN BY DATE APP
A
BURST MODE LOGIC
5 DIGIT BCD UP COUNTER
BURST TERMINATE DECODE LOGIC
TRIGGERING LOGIC
COUNTER LOAD LATCH
BURST CLOCK LOGIC
ONE SHOT
MANUAL TRIG RETURN LOGIC
MAN TRIG DEBOUNCE LOGIC
GEN BOARD(A3)
FRONT PANEL(A1)
FRONT PANEL ASSY(A1)
TTL VCC
74LS10
74LS00
74LS04
74LS30
74LS160
74LS00
SW1B (PERIOD)
TRIG
MAN TRIG
TRIG GATE INPUT
SW3 MAN TRIG
SW3-B, N.O.
SW3-B, N.C.
BCEN
BDIS
GATE
CONT
BURST
MGEN
N/C
1. ALL RESISTORS ARE IN OHMS. NOTE UNLESS OTHERWISE SPECIFIED
2. ALL CAPACITORS ARE IN MICRO-FARADS.
3. ALL DIODES ARE FD6666
4. LAST REF DESIGNATORS ARE R18, C9, CR4, U12 & J3
5. REFERENCE DESIGNATORS SHOWN ARE PARTIAL PREFIX WITH ASSEMBLY NUMBER A4.
BISHOP GRAPHICS/ACCUPRESS REORDER NO A-3394
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN
PROJENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°
DO NOT SCALE DWG
SCALE
DATE 4/81
WAVETEK SAN DIEGO, CALIFORNIA
TITLE SCHEMATIC BURST BOARD (A4)
MODEL NO 803
DWG NO 0103-10-5780
REV A
SYSTEM NUMB 23338
SHEET 1 OF 1

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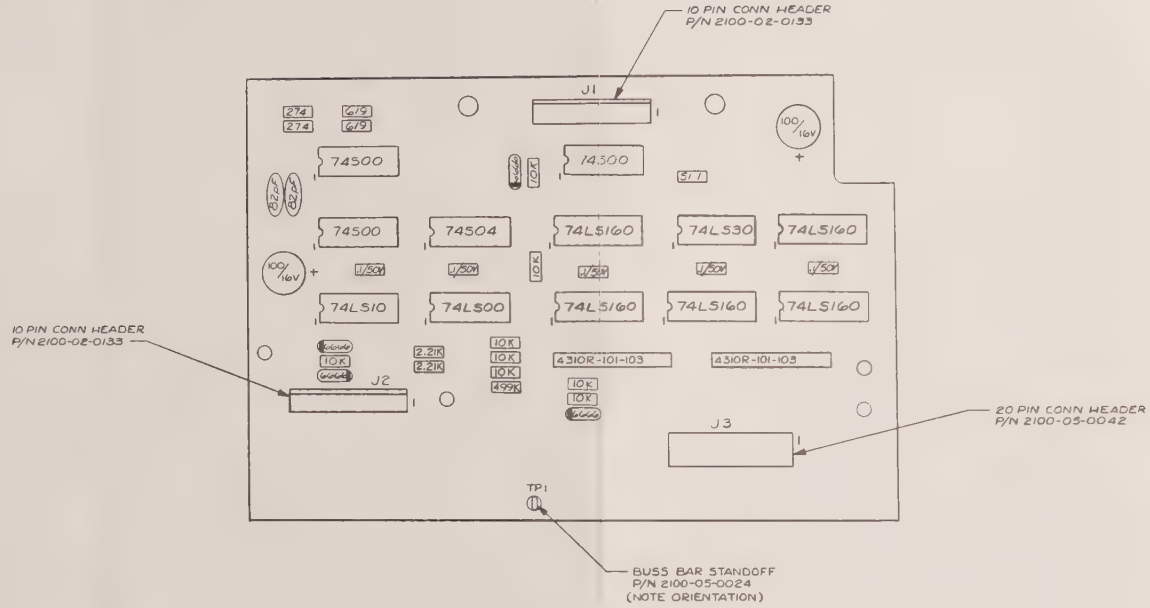
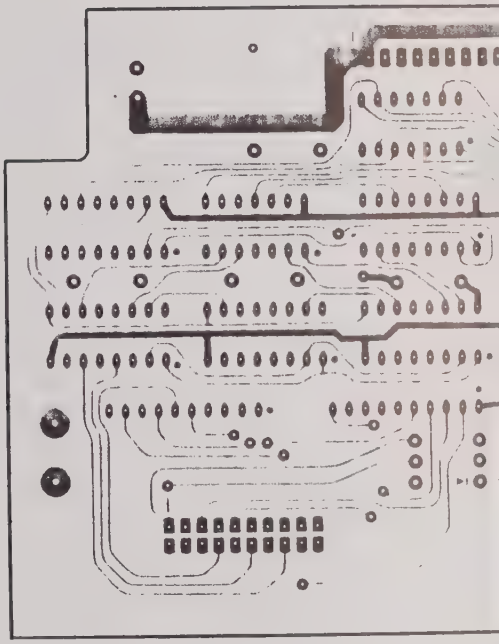
REV	ECN	BY	DATE	APP
A	3297	PW	8/1/82	DK



NOTE UNLESS OTHERWISE SPECIFIED

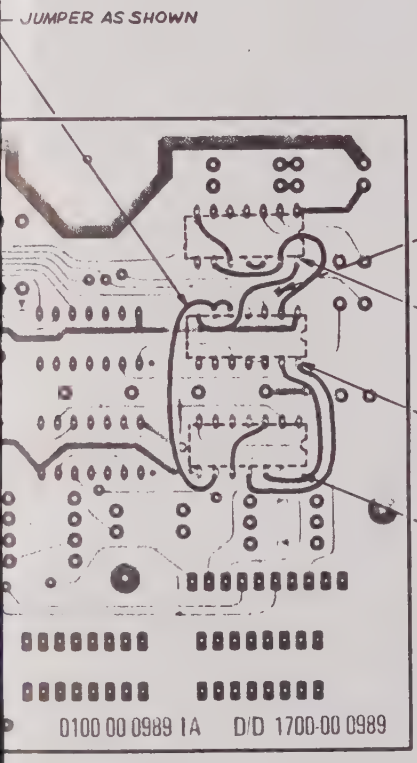
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 1-15-30	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ MGR	5-3-82	TITLE: ASSEMBLY, BURST BOARD (A4)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 803	DWG NO 0101-00-0989 REV A
	SCALE 2/1	CODE IDENT 23338	SHEET 1 OF 2

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP



MOD. INSTRUCTIONS

STEP	
1.	CUT LAND, BOTTOM OF BOARD, TO U3 PIN 13.
2.	JUMPER U3 PIN 2 TO U8 PIN 3.
3.	JUMPER U3 PIN 1 TO U8 PIN 4.
4.	JUMPER U8 PIN 12 TO U8 PIN 5.
5.	JUMPER U8 PIN 6 TO U3 PIN 9 TO U3 PIN 10.
6.	JUMPER U3 PIN 8 TO U1 PIN 1.
7.	JUMPER U1 PIN 5 TO U1 PIN 8.
8.	JUMPER U1 PIN 3 TO U1 PIN 4.
9.	JUMPER U1 PIN 2 TO U1 PIN 6 TO U3 PIN 13.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 8-10-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: ASSEMBLY BURST BOARD (A4) MOD.
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .020		
	DO NOT SCALE DWG	MODEL NO 803	DWG NO 0101-00-0989 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, BURST BD	0101-00-0989	WVTK	0101-00-0989	1
NONE	SCHEMATIC, BURST BD	0103-00-0989	WVTK	0103-00-0989	1
C4 C5 C6 C7 C8	CAP, CER, MON. .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	5
C2 C3	CAP, CER, 82PF, 1KV	DD-820	CRL	1500-08-2011	2
C1 C9	CAP, ELECT, 100MF/16V RADIAL LEAD, SP .20	CRE SERIES 100/16	CAPAR	1500-31-0111	2
NONE	BURST BOARD	1700-00-0989	WVTK	1700-00-0989	1
J1 J2	CONNECTOR, HEADER (10 PIN)	1-640456-0	AMP	2100-02-0133	2
TP1	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	1
J3	HEADER, 20 PIN	929836-01-10	AP	2100-05-0042	1
R10 R11 R13 R14 R15 R16 R6 R9	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	8
R7 R8	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	2
R1 R3	RES, MF, 1/8W, 1%, 274	RN55D-2740F	TRW	4701-03-2740	2
R12	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	1
R5	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	1
R2 R4	RES, MF, 1/8W, 1%, 619	RN55D-6190F	TRW	4701-03-6190	2
R17 R18	RES MODULE	4310R-101-103	BOURN	4770-00-0008	2

WAVETEK PARTS LIST	TITLE PCA: BURST	ASSEMBLY NO. 1100-00-0989 PAGE: 1	REV A

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR1 CR2 CR3 CR4	DIODE	1N4148	FAIR	4807-02-6666	4
U1 U2 U3	IC	74S00	TI	8000-74-0001	3
U9	IC	74LS00	TI	8000-74-0010	1
U4	IC, HEX INVERTER	74S04	TI	8000-74-0401	1
U8	IC	74LS10	TI	8000-74-1010	1
U6	IC	74LS30	SIG	8000-74-3010	1
U10 U11 U12 U5 U7	IC	74LS160	SIG	8007-41-6010	5

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